SHARP SERVICE MANUAL

CODE: 00ZPC4641SM-E

PERSONAL COMPUTER

PC-4641

MODEL PC-4602

CONTENTS

SHARP CORPORATION

CHAPTER 1. OVERVIEW

1. Scope

This manual is covered for PC4602 and PC4641 CPU and hard disk drive.
For detailed information on other auxiliary equipment and options (list following), please refer to the separate service manuals provided for each devices.

- Service-man Diagnostic Manual
- CRT adaptor (CE-451A)
- EP-ROM card (CE452B)
- MODEM card (CE451M)
- MFD unit (CE452F)
- EMS card (CE453B)
- Floppy disk drive (FD-235F)

2. Special service tools

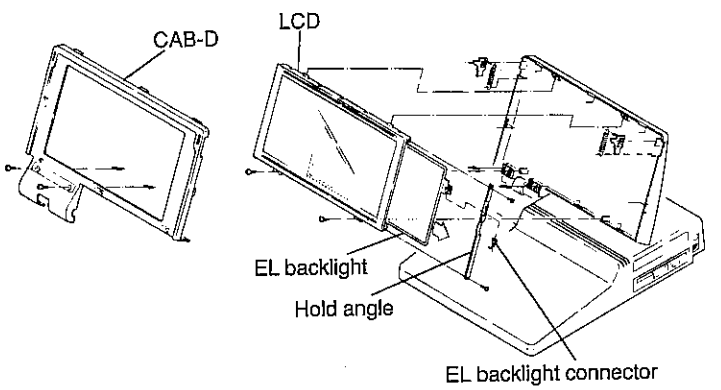
	Part code	Price Rank	Tool name
1	UKOGC3045CSZZ	BF	Service-man Diagnostic media
2	00G1490051603	CP	Alignment media
3	00G1490051701	CE	Level disk
4	UKOG-1055ACZZ	AV	Extension cable for FDD unit

3. Service method

1) Replacing the EL backlight

NOTE: The POWER switch must be turned off before replacing the EL backlight. Pay attention that a high voltage is on the EL backlight.

1. Remove the cosmetic sheet, then the CAB-D holding two screws.
2. Unfasten the cabinet-D from the cabinet-C after releasing latches at seven locations.
3. Unfasten the EL backlight connector.
4. Remove the LCD from the CAB-C (2 screws).
5. Remove the bracket from the LCD.
6. Slide the EL backlight towards right to remove. Then, replace it with a new one.



NOTE: Do not use the cosmetic sheet once removed. Be sure to use the new one.

2) HD INTERFACE AND HD DRIVE
The interface board and the HD drive unit can be replaced only in whole unit, but not in part. When they are diagnosed to be defective by the diagnostic program (UKOGC3045CSZZ), replace the whole unit of them.

4. Cautions

1) Although the CE-451A CRT adaptor board is an option for the PC-4600, it comes standard for the US version PC-4600. For more information about the wiring schematics and parts layout, refer to the CE-451A Service Manual (00ZCE451ASM-E).
2) Cosmetic sheet
Do not use the cosmetic sheet once removed. Be sure to use the new one.
3) Deposit of a paint dust on the back of the cabinet may fall on the PWB when the machine is disassembled and re-assembled for servicing and it may then cause a machine malfunction. To avoid this, the machine internal must be cleaned whenever the machine is disassembled.

CHAPTER 2. GENERAL INFORMATION

1. General information

PC-4600 series are compact and lightweight laptop computers. They pack the power and sophistication of desk-top models into the laptop size.

In order to attain the high performance, this computer accommodates large and high contrast Supertwist LCD with the EL backlight, 3-1/2" floppy disk drive, 3-1/2" hard disk drive, and well-packed 90-key full keyboard. The display provides clear test and graphics in 640 by 400 dots especially by supporting 4-shades of gray (tiling) and 8 x 16 dots (character box) characters.

Further, PC-4641 incorporates a 40MB hard disk drive in its unit and accomplish battery operation. The full-size step-sculptured keyboard provides 90 keys, enhancing the ease of use with separate numeric keypad, separate function and cursor keys.

The main unit includes i80188 compatible CPU running at 10MHz, socket for coprocessor, 640KB RAM standard expandable to 1.6MB, a serial interface, a parallel printer interface, an external FDD interface. The internal options include modem card with a serial interface (for US/Canada only), color/monochrome CRT adaptor, ROM disk card, and 1MB EMS memory card. The external expansions include 5-1/4" 360KB floppy disk drive unit and carrying case.

The newly revised original BIOS assures the execution of numerous applications with the combination of MS-DOS 3.3 operating system.

PC-4600 series consists of the following 2 models:

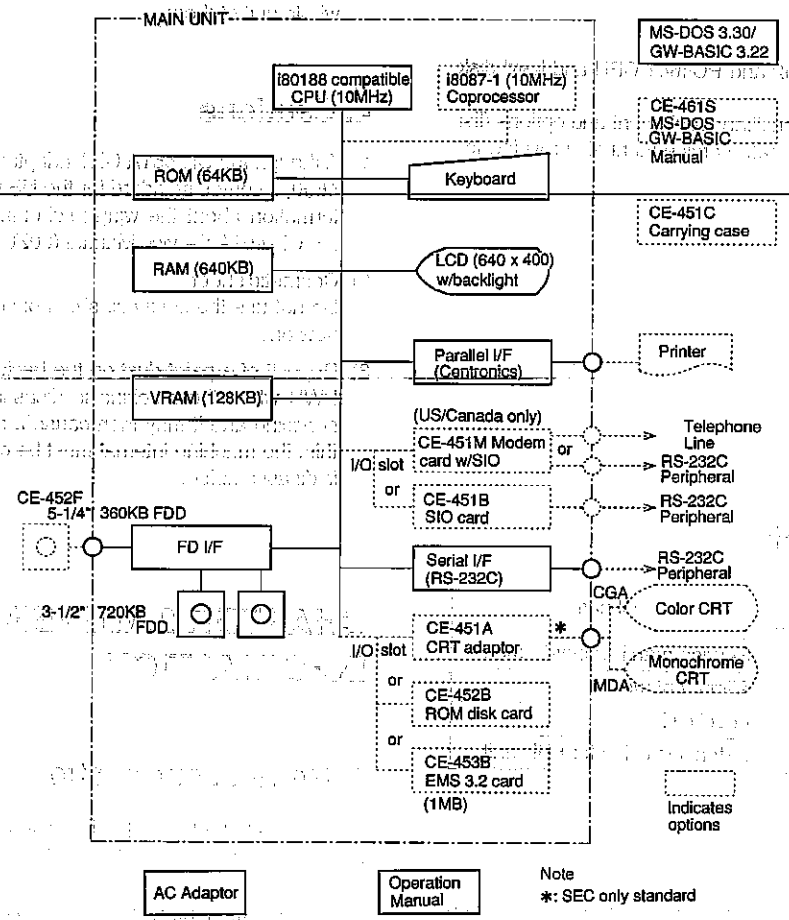
*PC-4602: 640KB RAM; two 3-1/2" 720KB FDDs; display w/ backlight; 90-key keyboard; serial interface; parallel interface; external 5-1/4" FDD (360KB) interface; MS-DOS 3.30/GW-BASIC 3.22

*PC-4641: 640KB RAM; a 3-1/2" 720KB FDD; a 40MB HDD; display w/ backlight; 90-key keyboard; serial interface; parallel interface; external 5-1/4" FDD (360KB) interface; MS-DOS 3.30/GW-BASIC 3.22

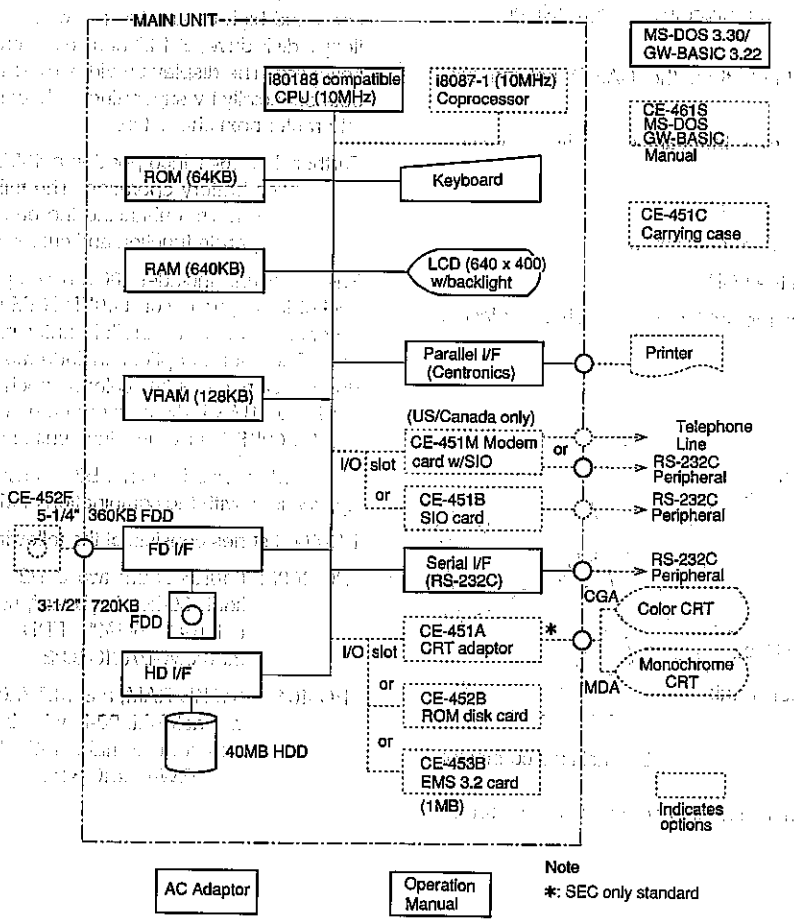
2. System Configuration

2-1. System block diagram

2-1-1. PC-4602



2-1-2. PC-4641



2-2. Specification

2-2-1. Main unit

CPU : NEC V40 (i80188 compatible)
CPU clock speed – 10MHz (7.16MHz when coprocessor is installed.)
System speed – Standard/Slow selectable on set-up menu

Coprocessor : Socket for i8087-1 (10MHz version)
NOTE: CPU clock speed is changed to 7.16MHz automatically when coprocessor is installed. When it is removed, CPU clock speed is changed to 10MHz automatically.

Memory : ROM – 64KB
including BIOS, set-up functions, CG, self check, etc
512K bits EP-ROM (27C512 type) x 1 piece
RAM – 640KB standard
256K bits (64K x 4 bits) DRAM x 20 pieces without parity
expandable up to 1.6MB with the optional 1MB EMS memory card (EMS 3.2)
VRAM – 128KB

Display : full-size large supertwist LCD with EL backlight
Text – 80 char. x 25 lines, 8 x 16 dots char. Box
Graphics – 640 x 400 pixels, 4-shades of gray (tiling)
Aspect ratio – 1:1
Emulation – CGA/MDA/AT&T 640 x 400 Graphics
Screen size – 233(w) x 147(h) mm
LCD active area – 230(w) x 144(h) mm
LCD contrast and backlight brightness are adjustable by each volume
Not detachable
90 – 129 degrees tilt angle adjustment
EL backlight
– white color
– life: Approx. 2,000 hours (until luminescent brightness becomes half)
– can be replaced by service man (service parts)

Data storage : PC-4602 – two side-mounted 3-1/2" 720KB FDD
upper: A drive, lower: B drive
PC-4641 – one side-mounted 3-1/2" 720KB FDD
one internal 3-1/2" 40MB HDD
upper: HDD (C drive), lower: FDD (A drive)
(FDD/HDD on the same side)
HDD – average access time: 45 msec
power save management:
can be set "Time-Out*" on set-up menu
Always ON/2 minutes/5 minutes/10 minutes
*: spindle motor of HDD will be controlled by the value of "Time-Out"

Keyboard : full-size 90-key step-sculpture keyboard
separate numeric keypad (with numeric +/– key)
separate cursor keys
10 programmable function keys
LEDs for Num Lock, Scroll Lock, and Caps Lock
Set-Up key for pop-up set-up menu
Cylindrical keytop
With click mechanizm
Not detachable

Interface : Serial (RS-232C) x 1 port (D-SUB 9 pin, male connector)
Parallel (Centronics) x 1 port (D-SUB 25 pin, female connector)
External 5-1/4" FDD (360KB) x 1 port (D-SUB 25 pin, female connecter)

I/O slot : Sharp proprietary slot x 2
– 1 slot for color/monochrome CRT adaptor, ROM disk card or
1MB EMS memory card (EMS 3.2)
– 1 slot for modem/SIO card (for US/Canada only) or SIO card

Power Supply : Rechargeable lead battery
– low battery warning
low battery indicator
alarm
AC adaptor
PC-4602/4641 : EA-452V
IN : local voltage
OUT : DC 9V, 2.5A
Dimension : 115(w) x 67(d) x 55(h) mm
Weight : Approx. 425g

Volume : LCD contrast volume
Backlight brightness volume

Switch : Power ON/OFF button (software switch)
5 dip switches

Dip Switch Label	Feature	Initial setting
1	System all reset ON/OFF	OFF
2	Not used	OFF
3	Speaker Volume LOW/HIGH	OFF (HIGH)
4	Speaker Control (without alarm) ON/OFF	ON
5	Alarm Control (Low Battery/Shut off Alarm) ON/OFF	ON

NOTE: User cannot use dip switches in PC-4600 for SEEG.
(for SEMKO, System all reset: Remove the lead battery)
Shut off alarm switch (alarm when upper cabinet is shut during power on.)

LED indicator : Power (green); low battery (red);
PC-4602 – drive A (green); drive B (green)
PC-4641 – floppy disk (green); hard disk (green)
Caps Lock (green); Num Lock (green); Scroll Lock (green)

Other : Carrying handle; speaker; display lock slide-switch x 2

Dimension : 12-1/8(w) x 13-3/4(d) x 3-1/4(h) inch
307(w) x 348(d) x 81(h) mm
(high: cushion rubber on the bottom cabinet included, without cushion rubber: 78mm)
NOTE: Above dimension is equal to PC-4500 series.
(with cushion rubber: 81(h) mm, without cushion rubber: 76(h) mm)

Weight : PC-4602 – 4.9kg (SEC) or 4.85kg (except for SEC)
PC-4641 – 5.5kg (SEC) or 5.45kg (except for SEC)
(with battery, without AC adaptor)
battery: Approx. 800g
AC adaptor (EA-452V): Approx. 425g

Software : MS-DOS 3.30/GW-BASIC 3.22

Manual : Operation Manual (MS-DOS/GW-BASIC quick reference included)
Optional MS-DOS and GW-BASIC manuals

2-2-2. Option

Internal Options:

CE-451A color/monochrome CRT adaptor
- color/monochrome 2 modes supported
  color: CGA (640 x 200 pixels)
  monochrome: MDA (720 x 350 pixels)
  color/monochrome mode is selected by set-up functions.
- 2 character sets (CG1/CG2) supported
  CG1: general
  CG2: Denmark/Norway
  CG1/CG2 is selected by short-pin switch on the card.

CE-451B SIO card
- Serial (RS-232C) x 1 port (D-SUB 25pin, male connector)
- dealer option

NOTE: Max. SIO 2 ports available when CE-451B installed.
1. Standard SIO (D-SUB 9pin, male connector)
2. SIO on the optional CE-451B SIO card (D-SUB 25pin, male connector)

CD-452B ROM disk card
- used as max. 768KB ROM disk
  6 sockets for 1M bits EP-ROM
  1M bits EP-ROM available on the market
- EP-ROM program in VAR
  utility software and technical document supplied by SHARP
- 2 types of EP-ROM (mask ROM compatible or JEDEC type) available on the market
  switchable by the slide-switch on the CE-452B card
- the following EP-ROM chips can be used;

	Mask-ROM compatible	JEDEC
Toshiba	TC571001D-20	TC571000D-20
NEC	μPD27C1000D-20	μPD27C1001D-20
Fujitsu	MBM27C1000-20	MBM27C1001-20
Mitsubishi	M5M27C100K-20	M5M27C101K-20

- with installation instructions

CE-453B EMS memory card
- 1MB EMS 3.2 memory card and EMS 3.2 software
- with operation manual

CE-451M modem card (for US/Canada only)
- mode/SIO 2 functions supported
  mode: 300/1200 BPS; Bell 103/212A;
  Hayes compatible command set
  SIO: RS-232C x 1 port (D-SUB 25 pin, male connector)
  modem/SIO function is selected by set-up functions
- dealer option
- with installation instructions

NOTE: Max. SIO 2 ports available when CE-451M is installed and used as a SIO.
1. Standard SIO (D-SUB 9 pin, male connector)
2. SIO on the optional CE-451M modem card (D-SUB 25 pin, male connector)

External options:

CE-452F 5-1/4" FDD unit (without SEEG)
- 5-1/4" FDD (360KB) x 1
- AC power
- with I/F cable

CE-451C carrying case
- soft case with shoulder strap

Manual:

CE-461S MS-DOS/GW-BASIC manual set
- MS-DOS 3.3 manual
- GW-BASIC 3.2 manual

SEEG options:

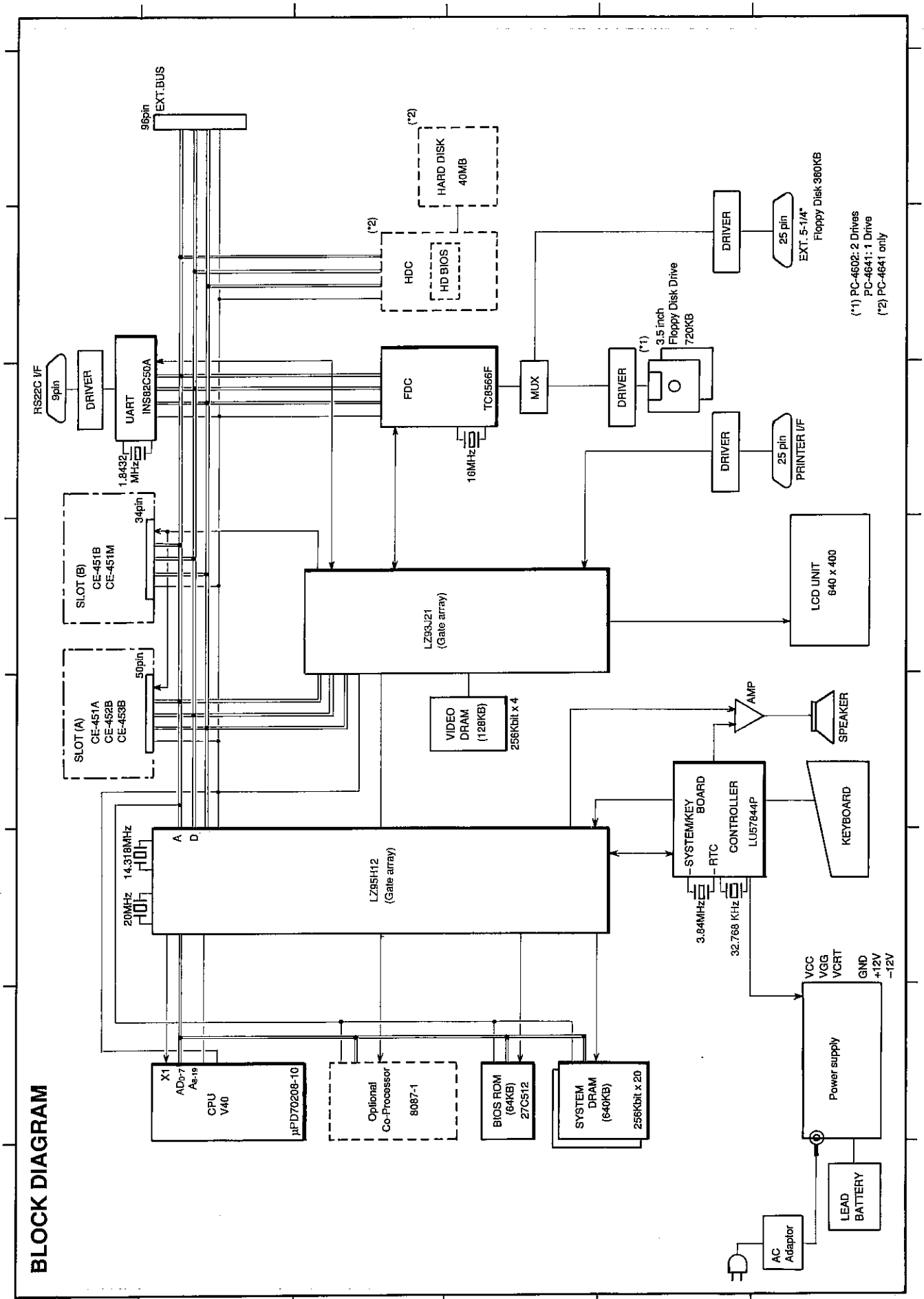
CE-460KE/F/W/M/S key top kit
- key top (E: 20, F: 25, W: 21, M: 21, S: 26 pieces)
- tool for pulling up the key top

CE-460SE/F/G/I operation manual
- PC-4602/4641 operation manual
  (E: English, F: French, G: German, I: Italian)

NOTE: CE-451A Color/monochrome CRT adaptor (CE-451A) is a standard for SEC only.

CHAPTER 3. MAIN BOARD OPERATION

BLOCK DIAGRAM



3-1. Memory and I/O map

3-1-1. Memory map for the PC-4600 system

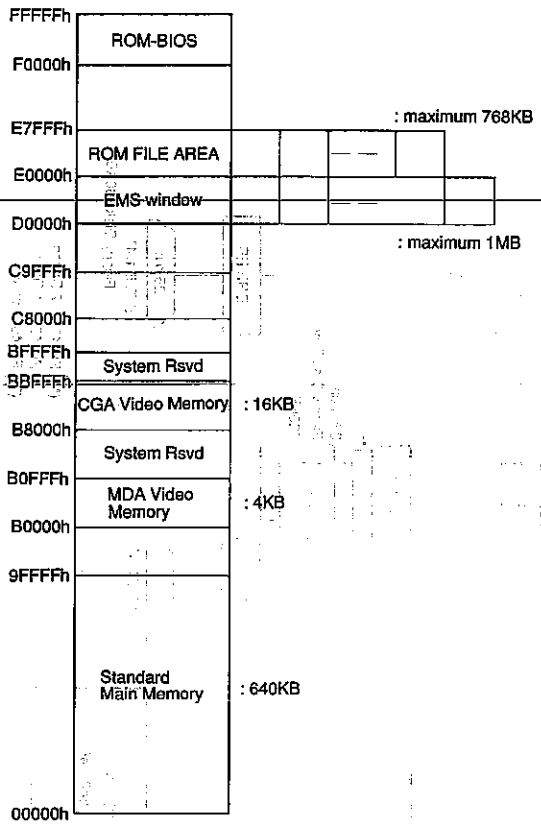


Fig. 3-1 Overall memory map

3-1-2. IO/MAP

Register	IO Address
Emulated DMA Controller	00H..0FH
V40DMA Controller	10H..1FH
Interrupt Controller	20H..3FH
System Timer	40H..5FH
PPI	60H..62H
NMI Mask	A0H..BFH
Asynchronous Communication (Secondary)	2F8H..2FFH
Hard Disk	320H..323H
Parallel Port	378H..37FH
Parallel Port	3BCH..3BEH
VIDEO IO	3B0H..3BBH
VIDEO IO	3BFH
VIDEO IO	3C0H..3CFH
VIDEO IO	3D0H..3DFH
FLOPPY DISK IO	3F0H..3F7H
Asynchronous Communication (Primary)	3F8H..3FFH
V40 System IO	FFF0H..FFFFH

3-2. Clock generator

The clock generator is included in LZ95H12, and connected with two crystal oscillators of 14.31818MHz and 20MHz.
The two clocks pass through the clock select circuit in LZ95H12, and one of them is outputted from X1 terminal to V40 X1 terminal. The details are shown in Fig. 3-2.

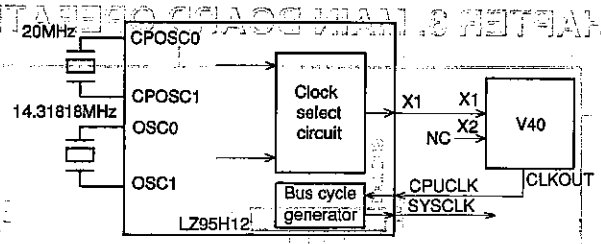
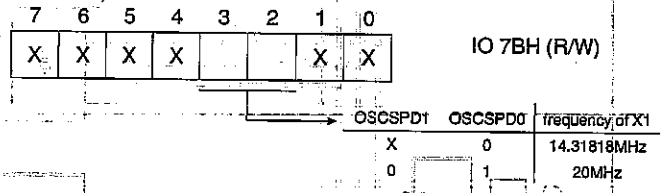


Fig. 3-2 Overall clock generate circuit

The frequency of the clock supplied from LZ95H12 X1 terminal to V40 is determined according to the states of bit 3 (OSCSPD1) and bit 2 (OSCSPD0) of the IO port (7BH) in LZ95H12 as shown below.



Assertion of the RESET signal will reset OSCSPD [0..1]. IF 8087 is not installed, ROM-BIOS sets OSCSPD0.
When setting OSCSPD0, the shift to frequency of 10MHz is made with no glitches, thus avoiding the need to reset the system.

3-3. Reset circuit

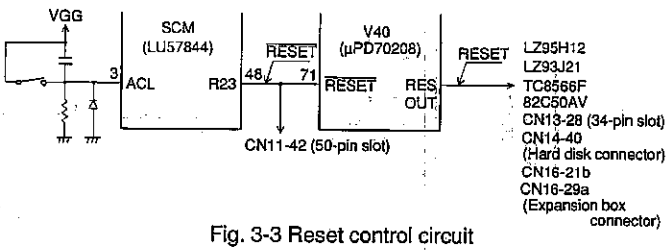


Fig. 3-3 Reset control circuit

The SCM can be reset in one of the following two ways.

1. When VGG turns on, a high state of signal is sent to the line ACL of the SCM from the differentiation circuitry composed of a capacitor and resistor.
2. When the dip switch-1, located at the lower side of the machine, set ON, it causes the ACL input high to reset the SCM. Operation starts when it turned off.

With depression of the ON/OFF switch while the machine is off or a hardware reset is given (simultaneous depression of CTRL, ALT, SETUP keys), VCC is turned active and $\overline{\text{RESET}}$ is forced high. The V40 synchronizes an async signal $\overline{\text{RESET}}$ with the internal clock and sends it out as an active high signal.

The former ($\overline{\text{RESET}}$) is sent to the V40 and 50-pin slot, and the latter (RESET) to the LZ95H12, LZ93J21, TC8566F, 82C50AV, 34-pin slot, hard disk controller, and the expansion box connector to reset with.

3-4. Interrupt control

Eight maskable interrupts and one non-maskable interrupt are provided.

- NMI is set high by the LZ95H12 when a specific I/O is accessed.
- Maskable interrupt may be caused in one of the following:

Number	Usage	Originating device
1	Keyboard	LZ95H12
3	Asynchronous communication (Secondary)	INS82C50A
4	Asynchronous communication (Primary)	
5	Hard disk	Hard disk controller
6	Floppy disk	TC8566F
7	Parallel printer	LZ93J21

3-5. Bus configuration

The PC-4600 system uses the forrowing two buses.

1) CPU (AD) bus

2) System Data (SD) bus

The bus configuration is shown in Figure 3-4.

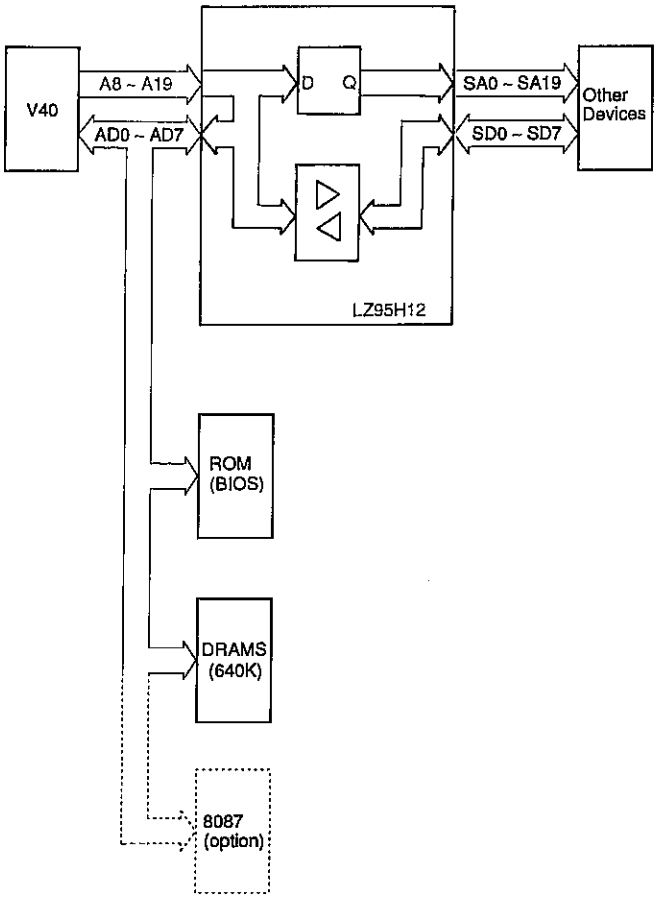


Fig. 3-4 Bus configuration

3-6. Memory

3-6-1. Block diagram

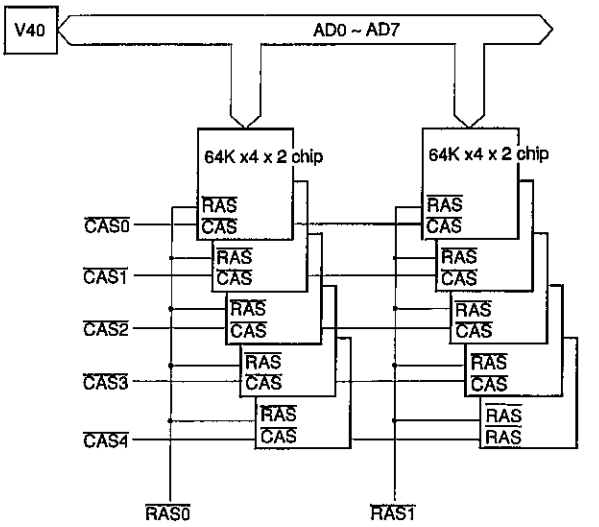


Fig. 3-5 RAM section block diagram

3-6-2. LZ95H12 address assignment

$\overline{RAS}$ and $\overline{CAS}$ are generated from LZ95H12. $\overline{RAS0}$ is set active if $\overline{RAS}$ is even address or $\overline{RAS1}$ active if $\overline{RAS}$ is odd address.

$\overline{CAS}$ signal is assigned to $\overline{CAS0}$ ~ $\overline{CAS4}$ as shown in Table 3-1.

Table 3-1

Input						Output								
A19	A18	A17	A16	A0	$\overline{REFRQ}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$	$\overline{CAS4}$	$\overline{ROMCE}$	
X	X	X	X	X	0	0	0	1	1	1	1	1	1	REFRESH
1	1	1	1	X	1	1	1	1	1	1	1	1	0	F0000H~FFFFFH
0	0	0	X	0	1	0	1	0	1	1	1	1	1	00000H~1FFFFH even
0	0	0	X	1	1	1	0	0	1	1	1	1	1	00000H~1FFFFH odd
0	0	1	X	0	1	0	1	1	0	1	1	1	1	20000H~3FFFFH even
0	0	1	X	1	1	1	0	1	0	1	1	1	1	20000H~3FFFFH odd
0	1	0	X	0	1	0	1	1	1	0	1	1	1	40000H~5FFFFH even
0	1	0	X	1	1	1	0	1	1	0	1	1	1	40000H~5FFFFH odd
0	1	1	X	0	1	0	1	1	1	1	0	1	1	60000H~7FFFFH even
0	1	1	X	1	1	1	0	1	1	1	0	1	1	60000H~7FFFFH odd
1	0	0	X	0	1	0	1	1	1	1	1	0	1	80000H~9FFFFH even
1	0	0	X	1	1	1	0	1	1	1	1	0	1	80000H~9FFFFH odd

3-6-3 Memory access timing

① Normal DRAM access

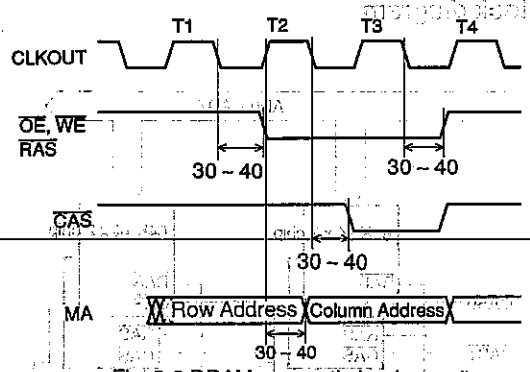
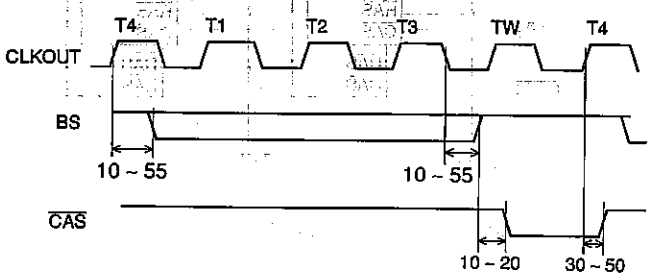


Fig. 3-6 DRAM access timing (normal)

② At DMA memory write



Same as ① for the timing of $\overline{OE}$, $\overline{WE}$, $\overline{RAS}$, and MA.

Fig. 3-7 DRAM access timing (DMA memory write)

③ ROM access

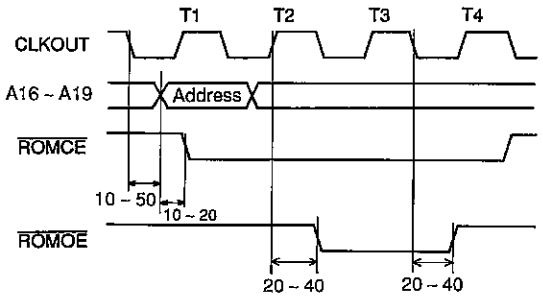


Fig. 3-8 ROM access timing

3-7. 8087 interface

The interface log of 8087 is stored in LZ95H12. The signal connection is shown in Fig. 3-9.

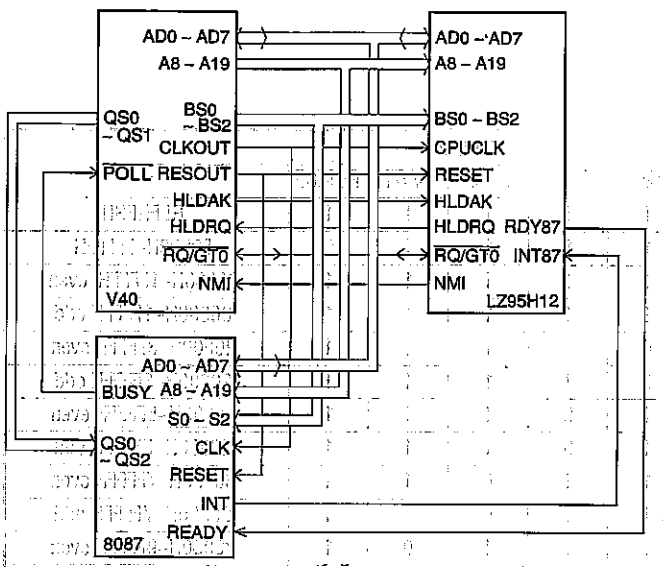


Fig. 3-9 8087 interface signal connection

3-8. READY control circuit

The signal READY (RDYV40) for V40 is controlled by LZ95H12. LZ95H12 and LZ95J21 control $\overline{EXTM}$, $\overline{EXTIO}$, SLOCYC, and READY signals for the devices accessed. LZ95H12 determines the bus cycle according to these signals, to control RDYV40. The block diagram is shown in Fig. 3-10.

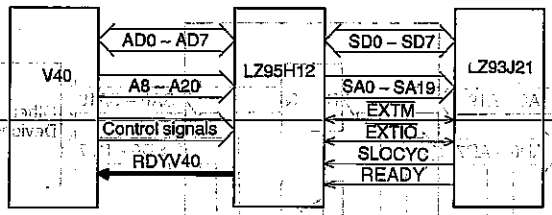


Fig. 3-10 Overall ready control signals

3-9. DMA control

Although the V40 has four DMA channels, two channels are used. DRQ2 and $\overline{DACK2}$ are used for controlling the floppy.

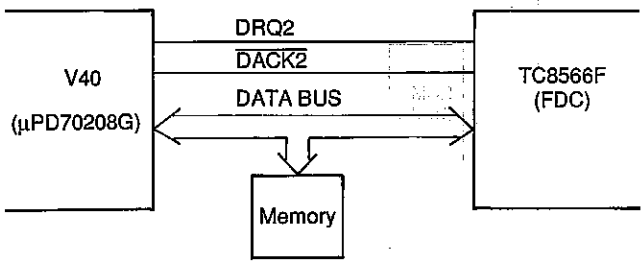


Fig. 3-11 Overall DMA control signals

When the V40 starts to DMA after setting the TC8566F register, the TC8566F sets DRQ2 high. After the V40 receives this signal, $\overline{DACK2}$ is set low to perform DMA transfer between the TC8566F and the memory.

DRQ3 and $\overline{DACK3}$ are used for controlling the hard disk. DRQ3 is supplied from the LSI in the hard disk controller. When DRQ3 becomes high, V40 makes $\overline{DACK3}$ low to perform DMA transfer between with the controller.

3-10. Bus cycle generator (including LZ95H12)

3-10-1. General

The LZ95H12 bus cycle generator produces the SYSCLK, ALE, STC, $\overline{SMRD}$, $\overline{SMWR}$, $\overline{SIORD}$ and $\overline{SIOWR}$ signals. It interprets the READY signal and drives the RDYV40 signal to control the number of wait states. The LZ95H12 determines the speed of the devices involved in the transfer. Devices are grouped into three speed categories:

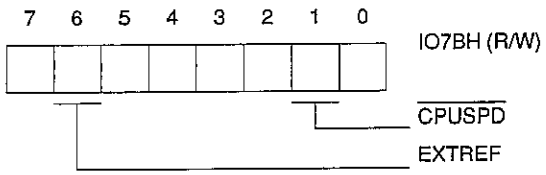
1. fast AD bus devices;
2. fast SD bus devices; and
3. slow SD bus devices.

Fast AD devices are the V40, the 8087, the LZ95H12, the system ROM the, system DRAM. Fast SD bus devices are those devices which are controlled by the LZ93J21 for which the SLOCYC signal is not asserted. This signal is sampled at the start of first T-cycle following the assertion of the $\overline{SMRD}$, $\overline{SMWR}$, $\overline{SIORD}$ or $\overline{SIOWR}$. At 7.16MHz, this occurs at the start of T3. At 10 MHz this occurs at the start of the first TW. All other devices are slow SD bus devices.

There are three speeds of non-refresh cycles: fast, medium and slow. Fast speed cycle execute with no wait states, except for IO NMI trapping cycles, which take nine T-cycles. Medium speed cycles may also insert wait states in response to a reset READY signal. A special extended medium speed cycle that drives SYSCLK from CPUCLK is also implemented. At 7.16 MHz, the minimum medium speed cycle takes 5 T-cycles. At 10 MHz, the minimum medium speed cycle takes 6 T-cycles. Medium and slow speed cycles have the same timing until SLOCYC is sampled.

If the $\overline{\text{CPUSPD}}$ (IO7BH bit 1) bit is set, the bus cycle generator will only generate slow speed memory cycles. This is done to accommodate programs using software timing loops. Assertion of the RESET signal will reset $\overline{\text{CPUSPD}}$. If $\overline{\text{CPUSPD}}$ is reset, then speed of the cycle is dependent on the slowest device involved. If the slowest device is a fast AD bus device then a fast speed cycle is generated. If the slowest device is a fast SD bus device, then a medium speed cycle is generated. Otherwise, a slow speed cycle is generated. When "speed: slow" is selected in the set up menu, $\overline{\text{CPUSPD}}$ = 1 (High)

There are two speeds for refresh cycle-fast and slow. If the EXTREF (IO7BH bit 6) bit is set, the bus cycle generator will generate a slow speed cycle. Thus DRAM on the SD bus may be refreshed. If EXTREF and $\overline{\text{CPUSPD}}$ are reset, then the bus cycle generator will generate a fast speed cycle. Thus any DRAM on the SD bus must provide its own refresh. Resetting EXTREF may result in as much as a 5% increase in system throughput. Assertion of the RESET signal will reset EXTREF. When the optional EMS card (CE-453B) is installed, EXTREF = 1 (High).



3-10-2. SYSCLK Generation

For 7.16 MHz cycles, CLKOUT drives SYSCLK.
For 10 MHz fast speed cycles, SYSCLK is set during T2 and is reset during the rest of the cycle. For 10 MHz medium speed cycles, SYSCLK is set during T2, the first TW and T4 and is reset during the rest of the cycle. For 10 MHz extended medium speed cycles, SYSCLK is set during T2 and driven by CPUCLK for the rest of the cycle. For 10 MHz slow speed cycles, SYSCLK is set during T2, during the odd TW's and during T4 and is reset during the rest of the cycle. There are always an even number of TW's in a 10 MHz slow speed cycle. For 10 MHz cycles, SYSCLK is always reset during TI's and interrupt acknowledge cycles.

3-10-3. $\overline{\text{SWRD}}$, $\overline{\text{SMWR}}$, $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ Generation

$\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ are not asserted during non-refresh cycles that access fast AD bus memory devices. $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ are not asserted during non-refresh cycles that access LZ95H12 internal IO devices or V40 internal private IO devices. $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ are asserted during accesses to emulated MDA/CGA IO addresses. $\overline{\text{SMRD}}$ and $\overline{\text{SIOWR}}$ are not asserted during fast refresh cycles.

For 7.16 MHz cycles, the $\overline{\text{SMRD}}$ and $\overline{\text{SIORD}}$ signals may be reset during T2, T3 and TW. These signals are set during the rest of the cycle. The same is true for $\overline{\text{SMWR}}$ and $\overline{\text{SIOWR}}$ during non-refresh, non-DMA cycles. For DMA memory write cycles, the $\overline{\text{SMWR}}$ signal may be reset during T3 and TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle. For refresh and DMA memory read cycles, the $\overline{\text{SIOWR}}$ signal may be reset during T3 and TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle.

For 10 MHz fast speed cycles, the $\overline{\text{SMRD}}$, $\overline{\text{SMWR}}$, $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ signals are set during the cycle. For 10 MHz medium speed cycles, the $\overline{\text{SMRD}}$ and $\overline{\text{SIORD}}$ signals may be reset during T3 and TW. They are set during the rest of the cycle. The same is true for $\overline{\text{SMWR}}$ and $\overline{\text{SIOWR}}$ during non-refresh, non-DMA cycles. For DMA memory write cycles, the $\overline{\text{SMWR}}$ signal may be reset during all TW's except the first half of the first TW $\overline{\text{SMWR}}$ is set during the rest of the cycle. For refresh and DMA memory read cycles, the $\overline{\text{SIOWR}}$ signal may be reset during all TW's except the first half of the first TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle. For 10 MHz slow speed cycles, the $\overline{\text{SMRD}}$ and $\overline{\text{SIORD}}$ signals may be reset during T3 and all TW's except the last TW. They are set during the rest of the cycle. The same is true for $\overline{\text{SMWR}}$ and $\overline{\text{SIOWR}}$ during non-refresh, non-DMA cycles. For DMA memory write cycles, the $\overline{\text{SMWR}}$ signal may be reset during all TW's except the first TW and last TW. $\overline{\text{SMWR}}$ is set during the rest of the cycle. For refresh and DMA memory read cycles, the $\overline{\text{SIOWR}}$ signal may be reset during all TW's except the first TW and last TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle.

3-10-4. READY Interpretation and RDYV40 Generation

During fast speed cycles RDYV40 is set. RDYV40 is set during T1 and TI.

For 7.16 MHz medium speed cycles, RDYV40 is reset during T2 and then READY drives RDYV40 during the rest of the cycle. For 7.16 MHz slow speed CPU/COP memory cycles, RDYV40 is reset during T2 and T3 and then RDYV40 is driven by READY during the rest of the cycle. For 7.16 MHz slow speed IO, refresh and DMA cycles, RDYV40 is reset during T2, T3 and the first two TW's and then RDYV40 is driven by READY during the rest of the cycle.

For 10 MHz medium speed cycles, RDYV40 is reset during T2 and T3 and then RDYV40 is driven by READY during the rest of the cycle. For 10 MHz slow speed CPU/COP memory cycles, RDYV40 is reset during T2, T3 and the first two TW's. READY is sampled at the start and the end of the odd TW's starting with the first TW. If READY is reset for either sample, then RDYV40 remains reset for two more T-cycles and READY is again sampled. If READY is set for both samples, then RDYV40 remains reset for two more T-cycles and is then set for the rest of the cycle. For 10 MHz slow speed CPU/COP IO, refresh and DMA cycles, RDYV40 is reset during T2, T3 and the first four TW's. READY is sampled at the start and the end of the odd TW's starting with the third TW. If READY is reset for either sample, then RDYV40 remains reset for two more T-cycles and READY is again sampled. If READY is set for both samples, then RDYV40 remains reset for two more T-cycles and is then set for the rest of the cycle.

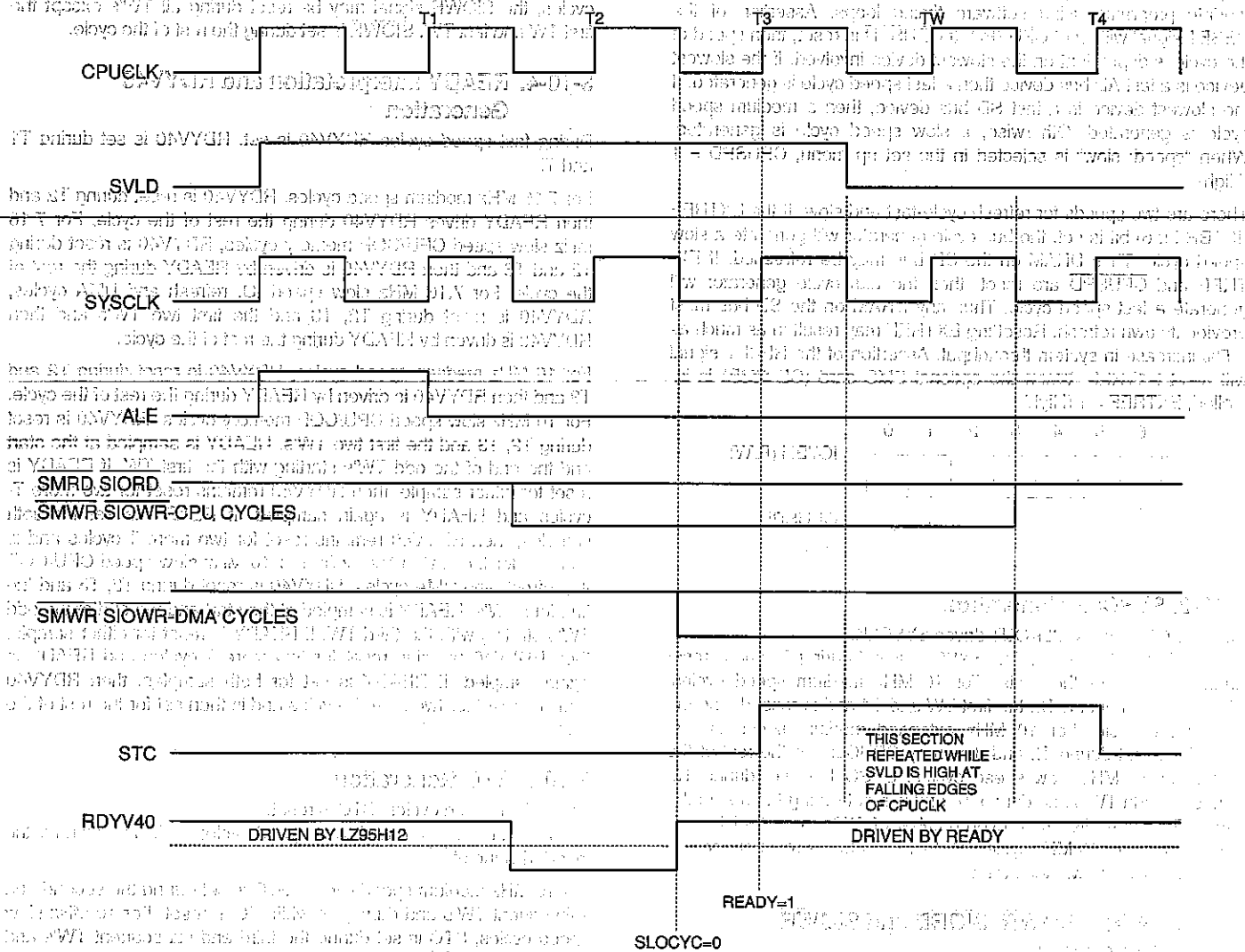
3-10-5. STC Generation

During fast speed cycles, STC is reset.
For 7.16 MHz medium and slow speed cycles, STC is driven by the inverted value of $\overline{\text{TC}}$.

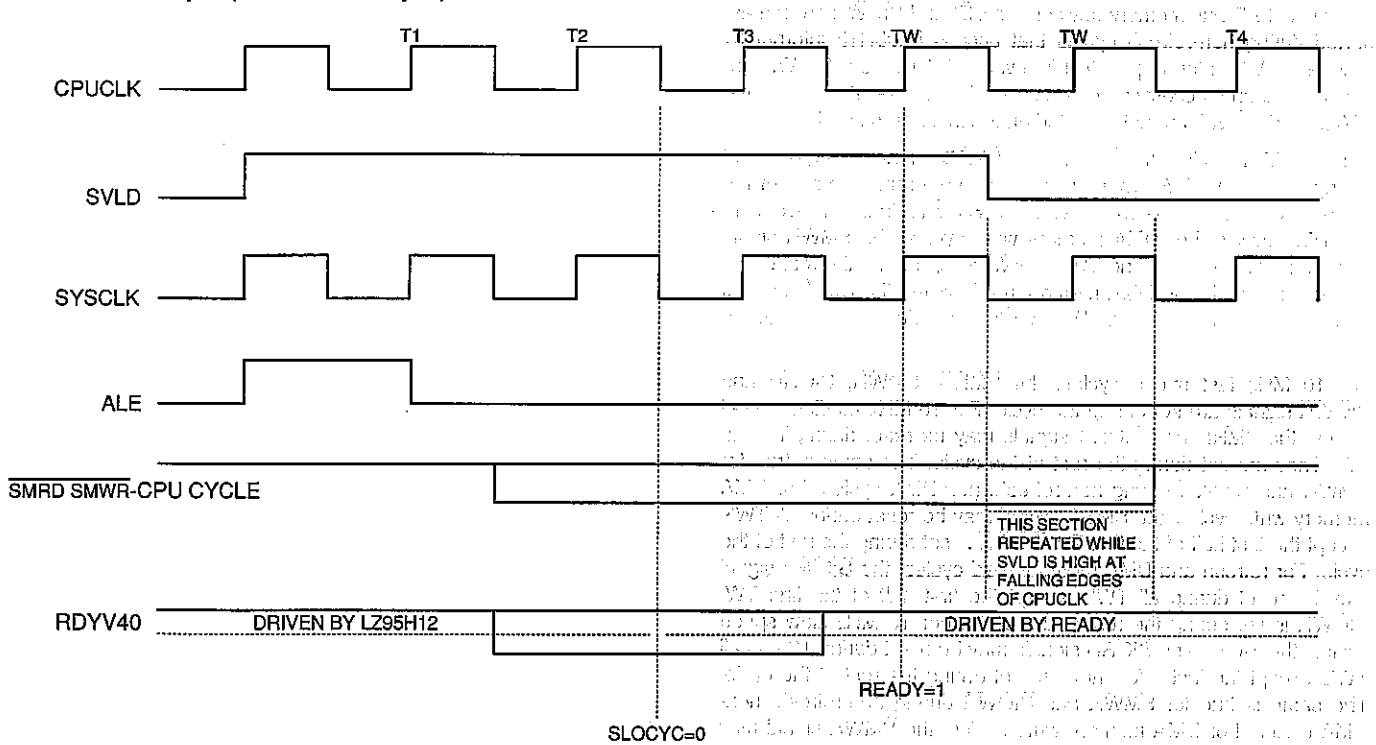
For 10 MHz medium speed cycles, STC is set during the second and subsequent TW's and during T4 while $\overline{\text{TC}}$ is reset. For 10 MHz slow speed cycles, STC is set during the third and subsequent TW's and during T4 while $\overline{\text{TC}}$ is reset. STC is reset during the rest of the cycle.

3-10-6. Timing chart

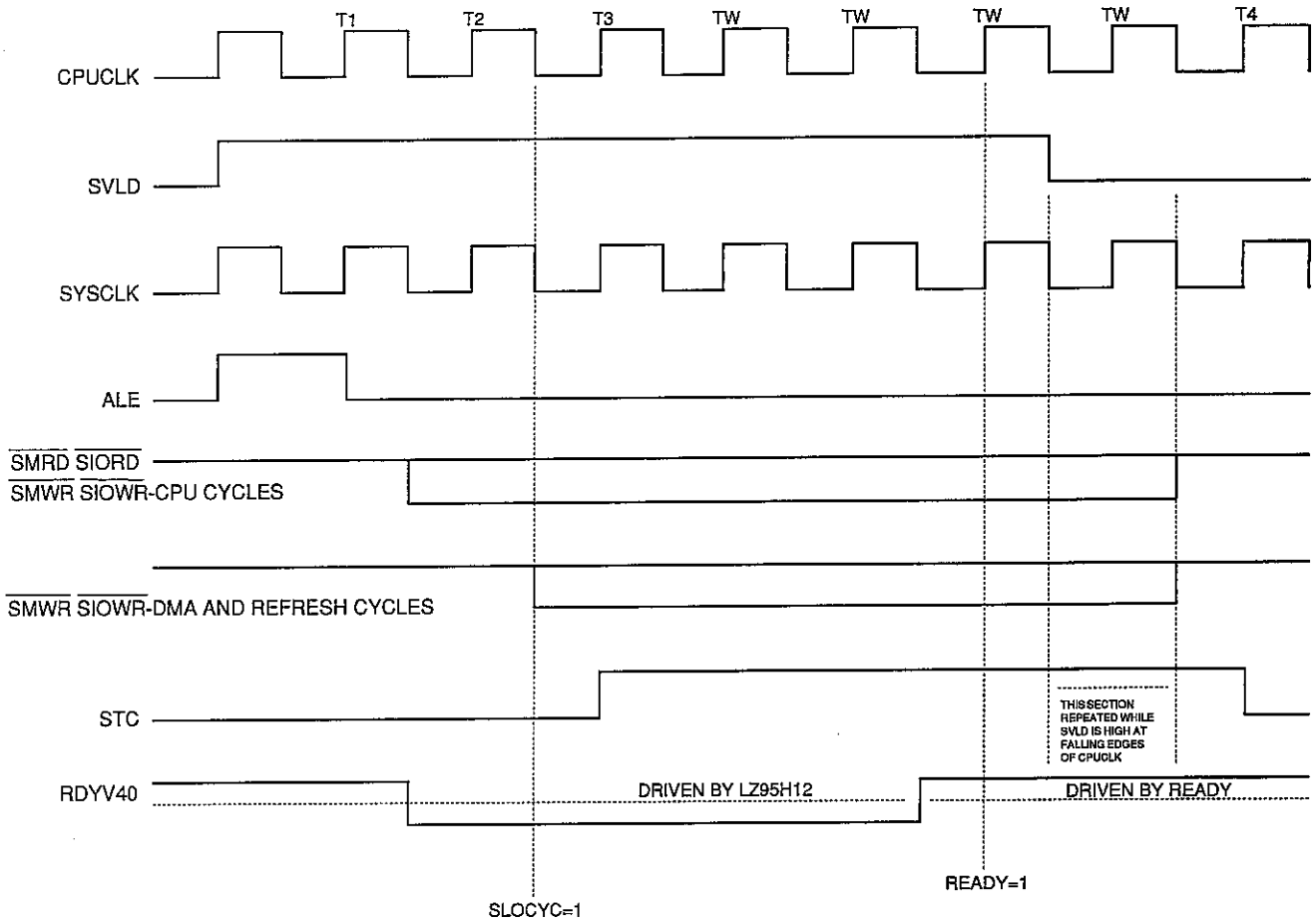
① 7.16 MHz MEDIUM cycle



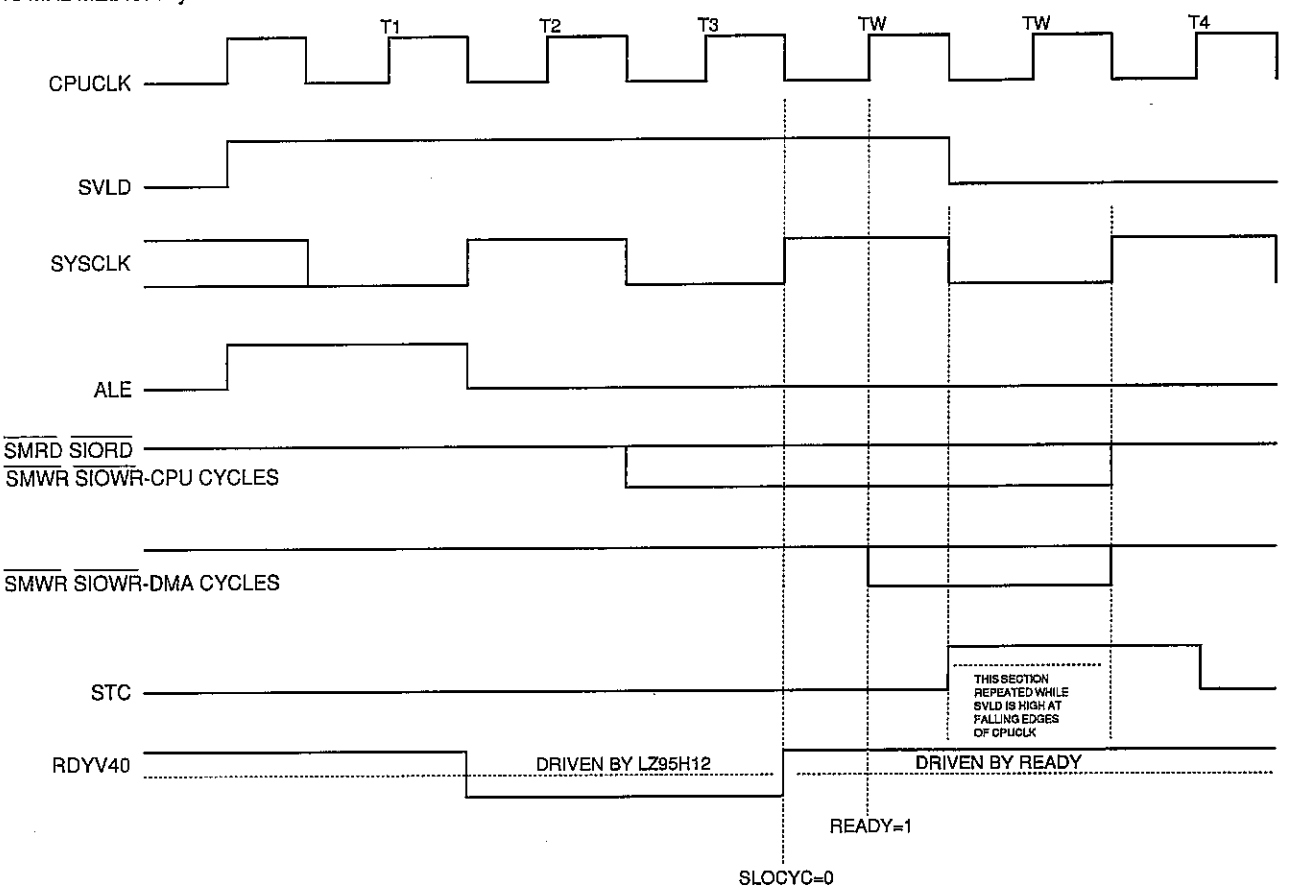
② 7.16 MHz SLOW cycle (CPU-MEMORY cycle)



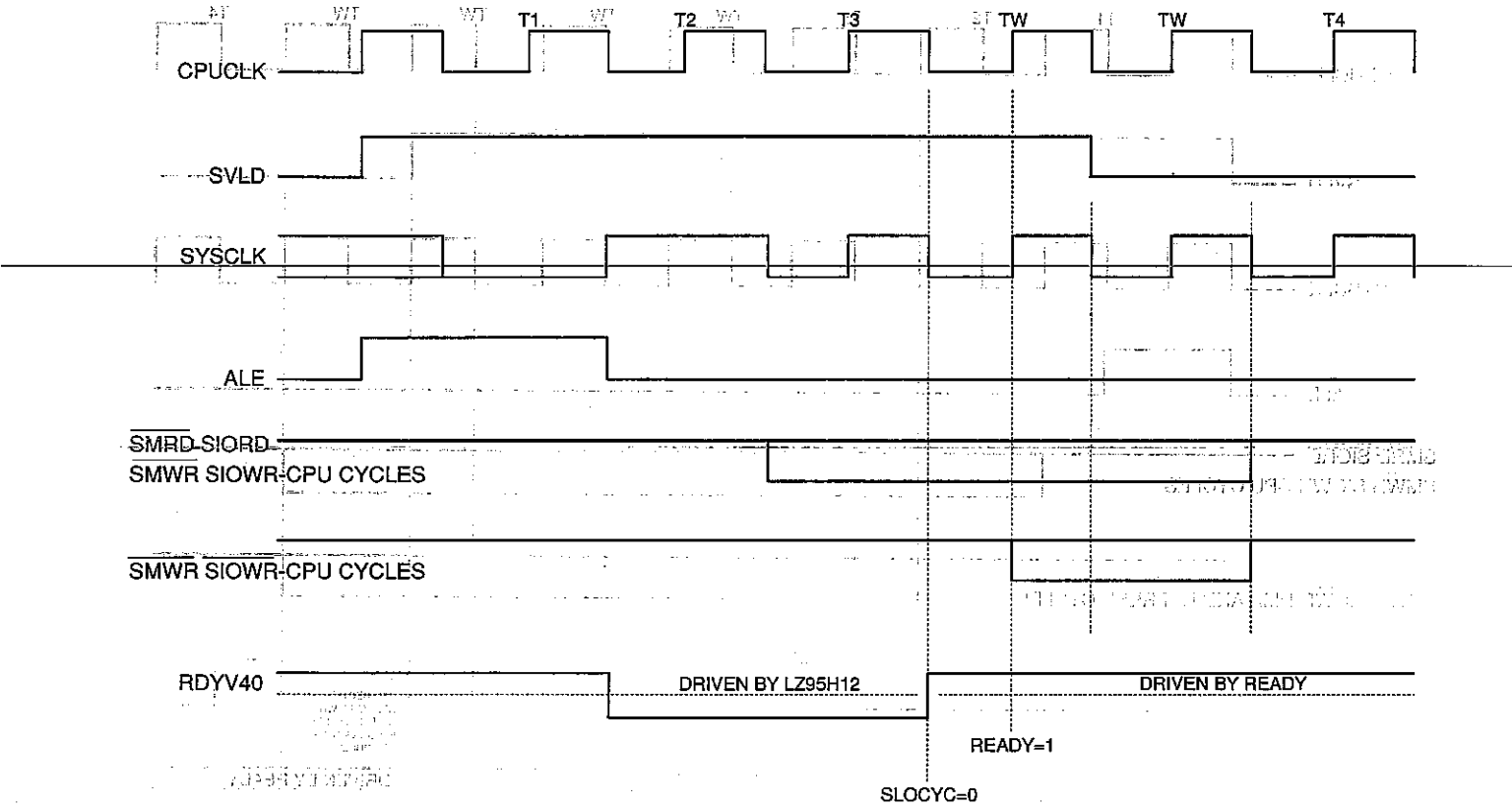
③ 7.16 MHz SLOW cycle (IO, DMA, REFRESH cycle)



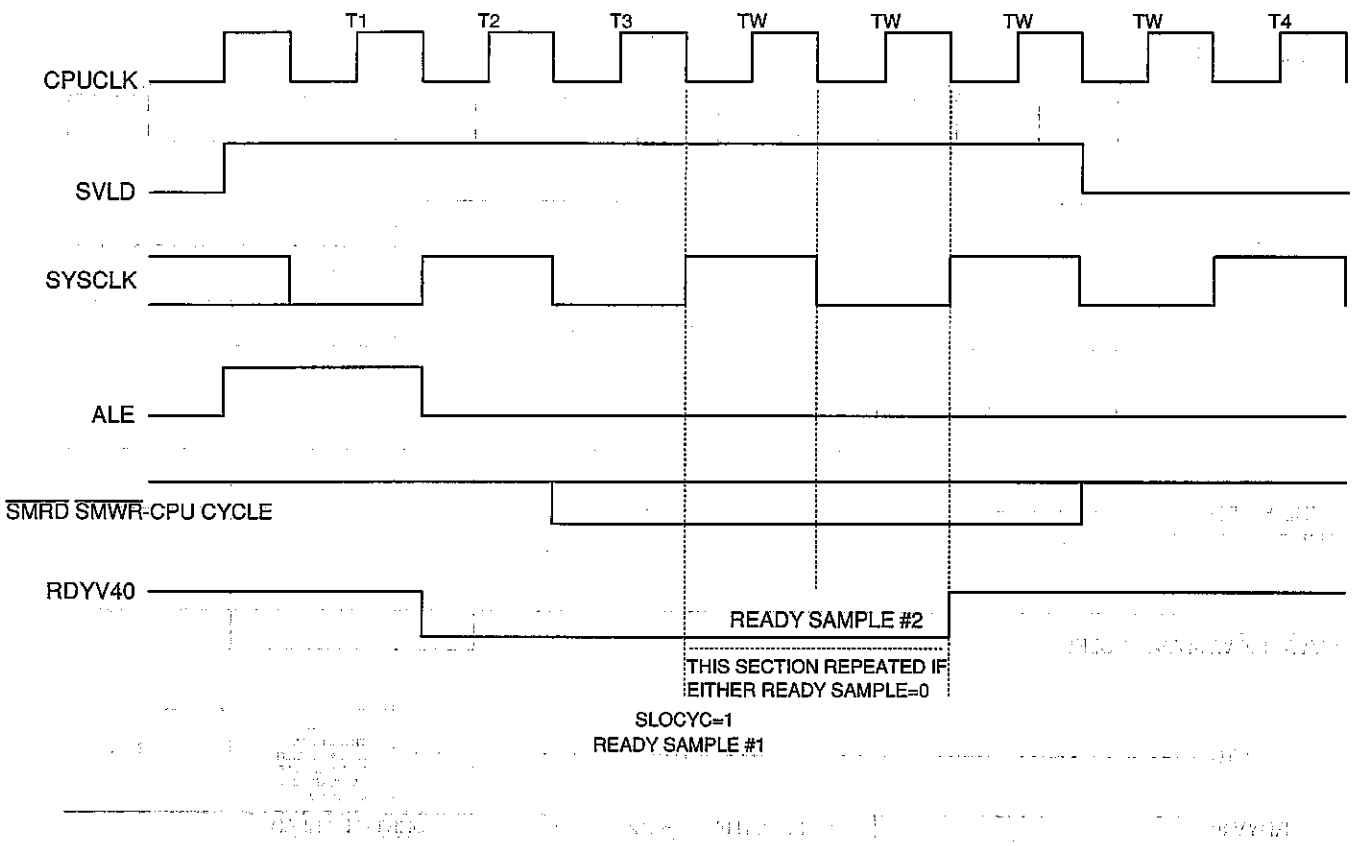
④ 10 MHz MEDIUM cycle



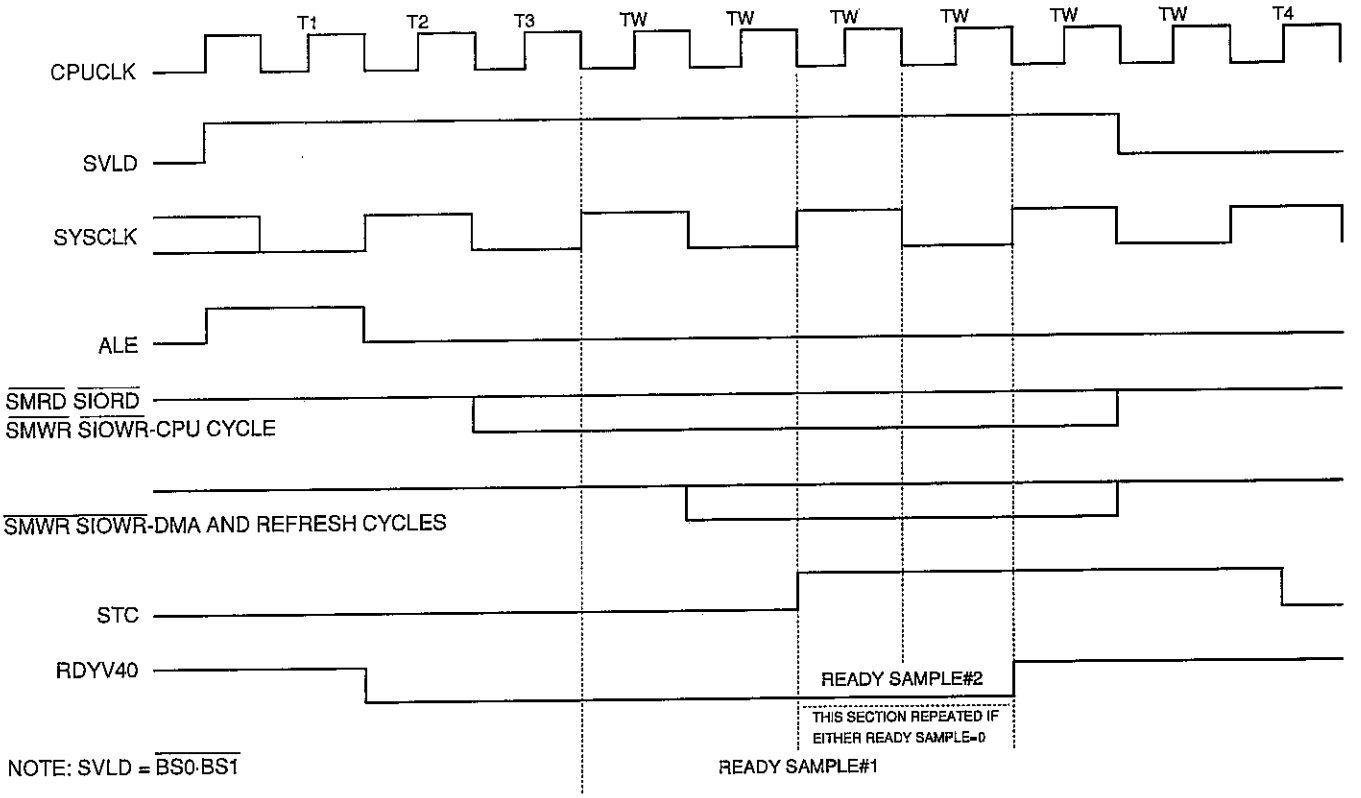
⑤ 10 MHz Extended MEDIUM cycle



⑥ 10 MHz SLOW cycle (CPU-MEMORY cycle)



⑦ 10 MHz SLOW cycle (IO, DMA, REFRESH cycle)



3-11. Printer interface

Fig. 3-12 shows a functional block diagram of the printer interface circuit. This circuit consists of the print data register, printer status port and printer control register.

The print data register, which is assigned at the I/O address 378H or 3BCH, stores data to be sent to the printer. The contents of this register can be read by the CPU at the I/O address 378H or 3BCH via the buffer.

The printer status port reads status information sent from the printer. This port is assigned at the I/O address 379H or 3BDH.

The printer control register stores control codes to be sent to the printer. This register assigned at the I/O address 37AH or 3BEH. Bit 4 of this register determines whether the $\overline{ACK}$ signal from the printer makes enable or disable as the CPU interrupt signal. When this bit is HIGH, interruption is enabled.

The contents of this register can be read by the CPU at the I/O address 37AH or 3BEH.

Assignment of the printer interface I/O address to either 37XH or 3BXH is dependent on the state of PPSEL (parallel port select bit 4) of the PC-4600 register CFR (Configuration Register) which is assigned to the I/O address 7FH. If PPSEL is 0, the printer interface I/O address is assigned to 3BXH. If PPSEL is 1, the address is assigned to 37XH.

It is possible to disable the standard printer adaptor by resetting PPS (bit 1) of the PCR (Planar Control Register) I/O address 65H which is normally set on.

Table 3-2 shows the printer I/O address definition.
Fig. 3-13 shows the printer timing chart.

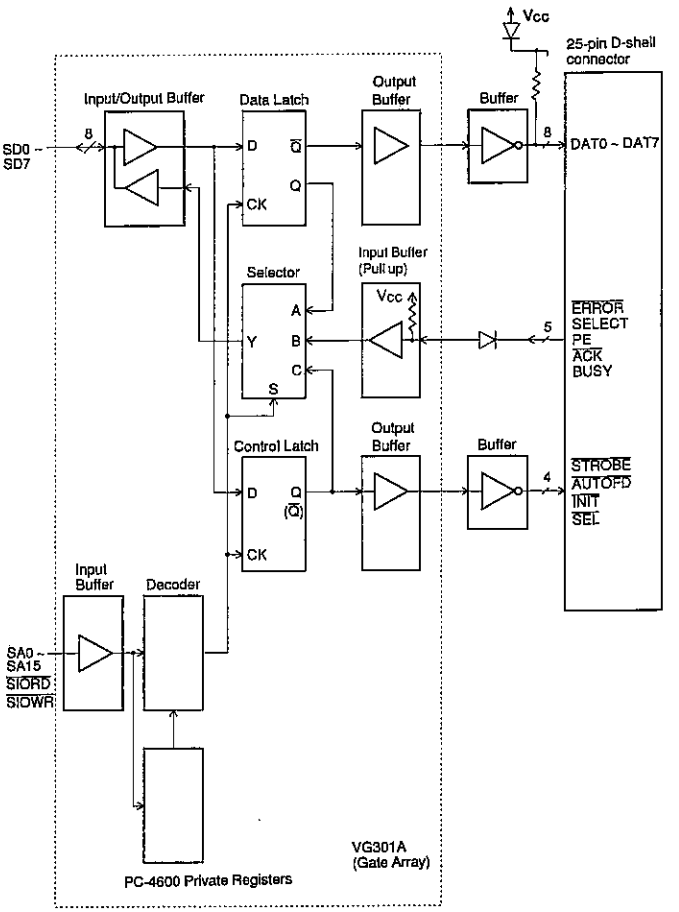


Fig. 3-12 Function block diagram

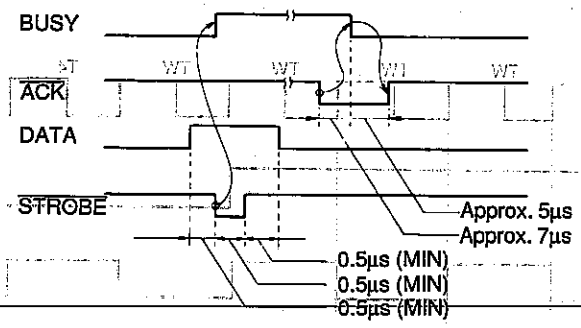


Fig. 3-13 Timing chart

I/O Address		Read/ Write	Bit	Description
65H		R/W	1	PPS. 1: Enables the standard printer adaptor (normally set 1).
7FH		R/W	4	PPSEL (Parallel Port Select) 0: Printer adaptor I/O address is assigned to 36XH. 1: Printer adaptor I/O address is assigned to 37XH.
	PPSEL	R/W	0	Print data 0 (LSB)
3BCH	0		1	Print data 1
			2	Print data 2
			3	Print data 3
			4	Print data 4
378H	1		5	Print data 5
			6	Print data 6
			7	Print data 7 (MSB)
	PPSEL	R	0	Not used (0 read)
3BDH	0		1	Not used (0 read)
			2	0 or 1 read
			3	$\overline{\text{ERROR}}$ read
379H	1		4	SELECT read
			5	PE read
			6	$\overline{\text{ACK}}$ read
			7	$\overline{\text{BUSY}}$ read
	PPSEL	R/W	0	STROBE written
3BEH	0		1	AUTOFD written
			2	$\overline{\text{INIT}}$ written
			3	SEL written
37AH	1		4	IRQENA, 1: Enables interrupt request.
			5	Not used (0 read)
			6	Not used (0 read)
			7	Not used (0 read)

Table 3-2 I/O address definition

3-12. Serial interface

As a standard, the PC-4600 has a serial interface which is assigned at the I/O address 3F8H through 3FFH or 2F8H through 2FFH.

Assignment of the serial interface I/O address to 3FXH or 2FXH is determined by the SCM (LU57832) output signal COM1/$\overline{2}$. When COM1/$\overline{2}$ is at a low, the serial interface I/O address is assigned to 3FXH. If high, the address is assigned to 2FXH.

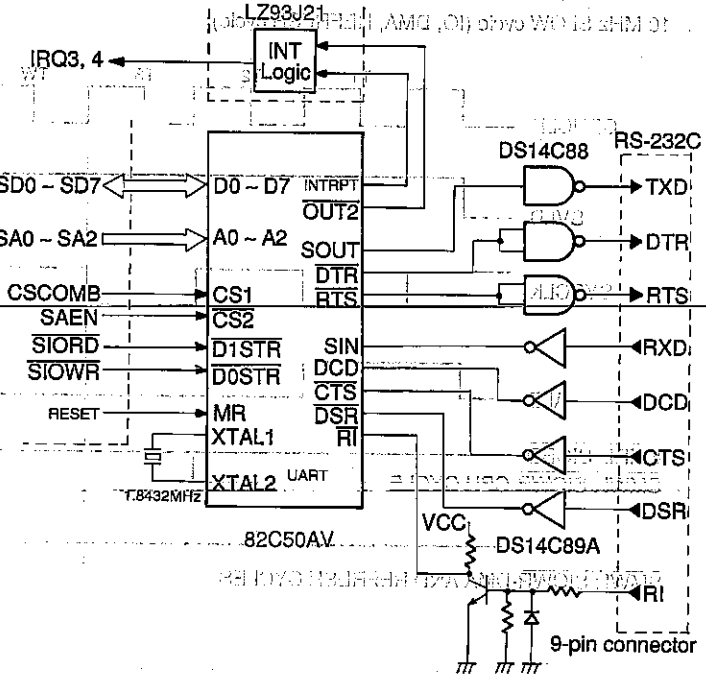


Fig. 3-14 Serial interface circuit

The serial interface circuit consists of transmitter DS14C88, receivers DS14C89A and the UART (INS82C50A). The convert TTL compatible signals sent from the UART to –12V to +12V signals conforming to the EIA standard, and output them via the RS-232 connector. The convert the EIA level reception signal to the TTL level and send it to the UART. The functional configuration of the UART is programmed by software via the data bus.

The UART performs a serial-to-parallel conversion of data characters received from a peripheral device or a MODEM, and a performs a parallel-to-serial conversion of data characters received from the CPU. The CPU can read the complete status of the UART any time during the functional operation. Status information includes the type and condition of the transfer operations performed by the UART, and provides error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator. Also the UART has a complete modem control capability and a processor-interrupt system that minimizes the computing time for handling the communications link.

When the CPU assigns one of the address 3F8H throu 3FFH or 2F8H throu 2FFH as an I/O address, the HIGH level CSCOMB signal sent from the VG301A (Gate Array) is emitted to the UART. The UART therr selects the internal register to be ZORC connected to the data bus according to the state of the DLAB (Divisor Latch Access Bit). The DLAB is bit 7 of the line control register. Table lists the state of registers indicates at each I/O address, and the table lists the bit assignment of each register.

I/O Address	A2	A1	A0	$\overline{\text{SIORD}}$	$\overline{\text{SIOWR}}$	DLAB	
3F8H or 2F8H	L	L	L	L	H	X	Receive buffer register
3F8H or 2F8H	L	L	L	H	L	X	Transmit holding register
3F8H or 2F8H	L	L	L	*	*	1	Divisor latch LSB
3F9H or 2F9H	L	L	H	*	*	1	Divisor latch LSB
3F9H or 2F9H	L	L	H	*	*	0	Interrupt enable register
3FAH or 2FAH	L	H	L	*	*	X	Interrupt identification register
3FBH or 2FBH	L	H	H	*	*	X	Line control register
3FCH or 2FCH	H	L	L	*	*	X	Modem control register
3FDH or 2FDH	H	L	H	*	*	X	Line status register
3FEH or 2FEH	H	H	L	*	*	X	Modem status register

*: $\overline{\text{SIORD}}$ becomes LOW at read operation
$\overline{\text{SIOWR}}$ becomes LOW at write operation
X: Not applicable.

I/O Address	Bit	Description
3F9H or 2F9H Interrupt enable register	0	H: Enable data
	1	H: Enable TX holding register empty interrupt
	2	H: Enable receive line status interrupt
	3	H: Enable modem status interrupt
	4 – 7	Always LOW
3FAH or 2FAH Interrupt identification register	0	H: No interrupt pending
	1	Interrupt identification bit 0
	2	Interrupt identification bit 1
	3 – 7	Always LOW
3FBH or 2FBH Line control register	0	Word length select bit 0
	1	Word length select bit 1
	2	Number of stop bit
	3	Parity enable
	4	Even parity select
	5	Stuck parity
	6	Set break
	7	Divisor latch access bit (DLAB)
3FCH or 2FCH Modem control register	0	Data terminal ready (DTR)
	1	Request to send (RTS)
	2	Out 1
	3	Out 2
	4	Loopback
	5 – 7	Always LOW
3FDH or 2FDH Line status register	0	Data ready (DR)
	1	Overrun error (OR)
	2	Parity error (PE)
	3	Framing error (FE)
	4	Break interrupt (BI)
	5	Transmit holding register empty (THRE)
	6	TX Shift empty (TSRE)
	7	Always LOW
3FEH or 2FEH Modem status register	0	Delta clear to send (DCTS)
	1	Delta data set ready (DDSR)
	2	Trailing edge ring indicator (TERI)
	3	Delta data carrier detect (DDCD)
	4	Clear to send (CTS)
	5	Data set ready (DSR)
	6	Ring indicator (RI)
	7	Delta carrier detect (DCD)

3-13. Speaker interface

A small, permanent magnet speaker is used in the sound system.
The speaker can be driven from one or two of sources.
It also can be driven by the SCM, CE-451M (modem).

- An LZ95H12 output bit
- A timer clock channel, output programmable within the function of the V40 timer. The timer gate can also be controlled by the LZ95H12 PPI output port.

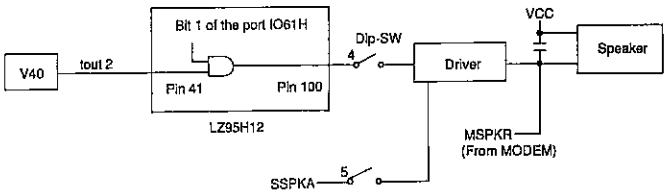


Fig. 3-15 Speaker controll circuit

3-14. RTC/CMOS RAM circuit

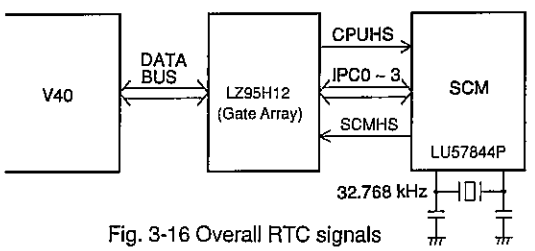


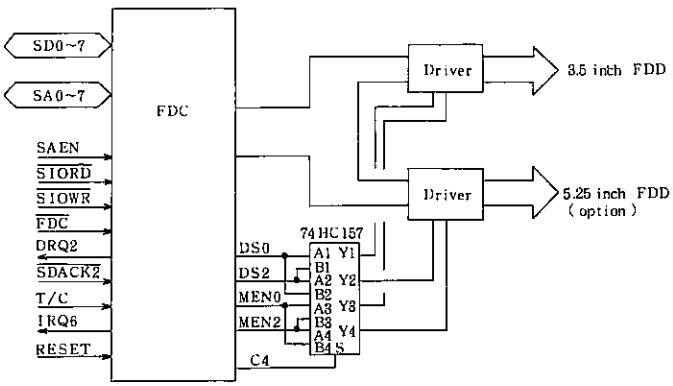
Fig. 3-16 Overall RTC signals

The SCM has a 32.768KHz crystal oscillator for the timer clock besides the program executing oscillator, and divided to cause an interrupt to the SCM itself at the given interval. Timer clock is counted in this interrupt routine and stored in the internal RAM (C-MOS RAM). This value can be read by the V40 via the LZ95H12 by means of handshaking.

For setup data are contained in SCM internal RTC and others, they can be read and written from V40 via LZ95H12 as handshaked with SCM, similar as RTC.

3-15. FDD interface circuit

The FDD interface circuit supports two floppy disk units at a maximum. Fig. 3-16 shows the block diagram. A TC8566F floppy disk controller is used to interface the floppy disk units with the CPU.



NOTE: The 74HC157 is used to select between the built-in 3.5 inch FDD and optional 5.25 inch FDD for drive A in the set-up menu.

Fig. 3-16 FDD interface block diagram

3-15-1. TC8566F floppy disk controller

The TC8566F floppy disk controller contains a VFO and peripheral logic circuit on a single chip.
Two control registers, main status register, and data register are on the chip. Table 3-3 shows the relation between address line and registers.

AEN	$\overline{CS}$	A7	A6	A5	A4	A3	A2	A1	A0	Function
H	X	X	X	X	X	X	X	X	X	No selection
X	H	X	X	X	X	X	X	X	X	
X	X	L	X	X	X	X	X	X	X	
X	X	X	L	X	X	X	X	X	X	
X	X	X	X	L	X	X	X	X	X	
X	X	X	X	X	L	X	X	X	X	
X	X	X	X	X	X	H	X	X	X	
L	L	H	H	H	H	L	L	L	L	Prohibit
L	L	H	H	H	H	L	L	L	H	
L	L	H	H	H	H	L	L	H	L	Control register-0
L	L	H	H	H	H	L	L	H	H	Control register-1
L	L	H	H	H	H	L	H	L	L	Main status register
L	L	H	H	H	H	L	H	L	H	Data register
L	L	H	H	H	H	L	H	H	L	No selection
L	L	H	H	H	H	L	H	H	H	

Table 3-3

3-15-1-1. Control register-0

This an 8-bit write only register.

Bit position	Symbol	Name	Significance
D7	MEN3	Motor enable-3	Control bit to control the motor in the No. 3 drive unit.
D6	MEN2	Motor enable-2	Control bit to control the motor in the No. 2 drive unit.
D5	MEN1	Motor enable-1	Control bit to control the motor in the No. 1 drive unit.
D4	MEN0	Motor enable-0	Control bit to control the motor in the No. 0 drive unit.
D3	ENID	Enable INT & DMA request	Used to set INTRQ and DRQ2 into effect. When this bit is at a low. INTRQ and DRQ2 stay inactive.
D2	$\overline{FRST}$	Not FDC reset	Used to reset the internal FDC. When this bit is 0, the FDC block is reset.
D1	DSB	Drive select B	Used to select FDC. The following is selected with DSB and DSA. (0, 0): No. 0 drive unit (0, 1): No. 1 drive unit (1, 0): No. 2 drive unit (1, 1): No. 3 drive unit But, if CDS is low, those bits are not in effect and bits are not in effect and the internal FDC select signal becomes effective. All bits will be cleared when RESET is set high.
D0	DSA	Drive select A	

All bits will be cleared when RESET is set high.

Table 3-4

3-15-1-2. Control register-1

This an 8-bit write only register.

Bit position	Symbol	Name	Significance
D3	C3	Control-5	These bits are open to user. Bit state appears on C5 and C4. If C4 is connected with MIN, for instance, the mini-floppy disk can be changed to the standard floppy disk by means of software.
D4	C4	Control-4	
D2	SBM	Standby mode	This bit indicates standby mode. Standby mode would not occur when this bit is at 0.
D0	FDCTC	FDC terminal counter	Used to control the FDC terminal count. When data transfer is terminated in the non-DMA mode, the terminal count is sent to the internal FDC block in reference to this bit.

Table 3-5

All bits will be cleared when RESET is set high. For data bus, D7, D5, D3, D1, are bit enable signal for D6, D4, D2, and D0, it is possible to change bit independently. For instance, writing 03H changes only FDCTC to 1 without changing the contents of C6, C4, and SBM.

3-15-2. Interfacing the FDC register with CPU

Interfacing the FDC register with CPU

The FDC has two registers which can be accessed by the main system processor. The one is main status register and the other is data register. The main status register indicates the FDC status information and can be accessed at any time. The 8-bit data register stores data, command, parameter, and FDD status. Data byte is written in the data register or read from the data register for programming or to obtain the results after command execution. The main status register is read only to facilitate data transfer between the FDC and the processor. The following shows the relation among the main status register, data register, $\overline{IOR}$, $\overline{IOW}$, and $\overline{CS}$.

Condition: A7=A6=A5=A4=A2=1, A3=A1=0, AEN=0

$\overline{CS}$	A0	$\overline{IOR}$	$\overline{IOW}$	Function
Low	Low	Low	Low	Prohibited
Low	Low	Low	High	Main status register read
Low	Low	High	Low	Prohibited
Low	High	Low	Low	Prohibited
Low	High	Low	High	Data register read
Low	High	High	Low	Data register write

Table 3-6

Each main status register bit is defined as in Table 3-7.
The main status register bits, RQM and DIO, indicate whether the data register is ready or which direction data are on the data bus.

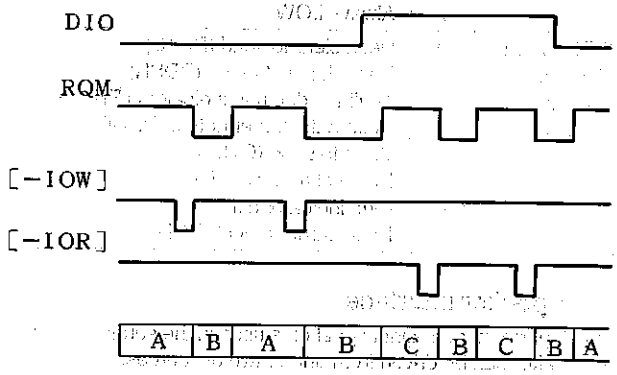


Fig. 3-17 Main status register timing

A (DIO=low, RQM=high):
Data register is enabled to write by the processor.
B (RQM=low)
Data register is not ready.
C (DIO=high, RQM=high)
Data register is read by the processor and a next data byte is already on.

Bit Position	Symbol	Name	Significance
D7	RQM	Request for master	Indicates that data are sent to the processor from the data register, or it is ready to receive data from the processor.
D6	DIO	Data input/output	Indicates data transfer direction when transferring data between the data register and the process or. A high on this line indicates that data are transferred from the data register to the processor. A low on this line indicates that data are transferred from the processor to the data register.
D5	NDM	Non-DMA mode	Indicates that the FDC is in the non-DMA mode. This bit can be active only in the execution phase of the non-DMA mode. A low on this line indicates that the execution phase has been completed.
D4	CB	FDC busy	This bit is set when a read-wirte related command is in execution or during execution of command phase or result phase.
D3	D3B	FDD3 busy	Indicates that the NO. 3 drive is in the seek mode.
D2	D2B	FDD2 busy	Indicates that the NO. 2 drive is in the seek mode.
D1	D1B	FDD1 busy	Indicates that the NO. 1 drive is in the seek mode.
D0	D0B	FDD0 busy	Indicates that the NO. 0 drive is in the seek mode.

Table 3-7. Main status register

The FDC may execute 15 different commands. Execution takes place with a multiple byte transfer by the processor, and results after command execution is indicates after multiple byte transfer to the processor. For multiple number of bytes are transferred between the FDC and the processor, it may be assumed to constitute the following blocks.

Command phase:

The FDC receives from the processor information required for the given operation.

Execution phase:

The FDC executes the given command.

Result phase:

After completion of the operation, the result status information are sent to the processor.

During execution of command phase and result phase, the processor needs to read the main status register before the byte information is written in the data register or read byte information from the data register. In order to write command and parameter bytes in the FDC, the main status register bit D7 must be high and bit D5 low. For majority of commands requires a multiple bytes, the main status register must be read before transferring bytes to the FDC. Also, the main status register bits D7 and D5 must be high before reading bytes from the data register during execution of the result phase. For the command phase and result phase, the main status register must be read before transferring bytes to the FDC, but may not be required necessarily for the execution phase. When the FDC is in the non-DMA mode, receive of data bytes (when the FDC is reading data from the FDD), INT (INT=1) is caused. If $\overline{IOR}$ ($\overline{IOR}$=0) is issued, it not only send data on the data bus, INT may also be reset. However, if the processor may not be fast enough to handle the interrupt (within 13μs in the MFM mode), the main status register is interrogated. The bit D7 (RQM) function as INT. In the same manner, INT may be reset with $\overline{IOW}$ while write command is in execution.

INT is not issued while the execution phase is being executed when the FDC is in the DMA mode. The FDC issues DRQ (DMA request) when data bytes are ready, to which the controller set $\overline{DAC}$ low (DMA acknowledge) and $\overline{IOR}$ low to respond to it. DRQ is reset when DMA acknowledge is set low for a read related command. For a write related command, $\overline{IOW}$ functions the same as $\overline{IOR}$. An interrupt is request upon completion of the execution phase (TC received) which indicates the start of the result phase. After reading the first data byte in the result phase, INT is forced to reset. In the result phase, all data bytes shown in the command list must be read. For instance, in the result phase of read data command, there are seven data bytes. In order to finish the read data command, these all seven data bytes must be read. Otherwise, the FDC may not receive a new command. For other commands, all data bytes must have been read in the result phase. The FDC has five status registers. The above mentioned main status register may be read at any time by the procesor. Four result status registers (ST0, ST1, ST2, ST3) can be used only in the result phase and can be read at the termination of command. Size of the result status register depends on the command executed. Sequence of data bytes sent to the FDC in the command phase and data bytes read from the FDC in the result phase is as shown in the command list. In other words, a command code must be first sent, to be followed by other bytes in the given order. So, nothing could be short for the command phase and the result phase. When the last data byte of the command phase is sent to the FDC, the execution phase takes place automatically. Similarly, after reading the last data byte in the result phase, the command automatically terminates and the FDC becomes ready to accept a next command.

3-16. Keyboard interface

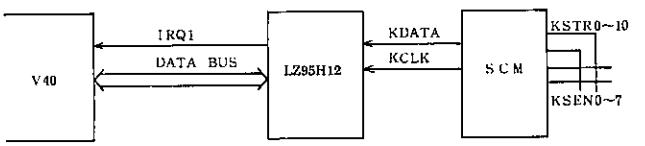
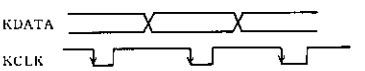


Fig. 3-18 Overall key signals

The SCM issues strobe through KSTR0–10 at every 6ms to scan the level on KSEN0–7 to sense key depression. The code is sent to the LZ95H12 on KDATA with a clock on KCLK. The following shows its timing.



After receiving the code in the shift register, the LZ95H12 turns IRQ1 high with which the V40 read the data from the LZ95H12.

(2) Keyboard LEDs (CAPS LOCK, NUM LOCK, SCRL LOCK)

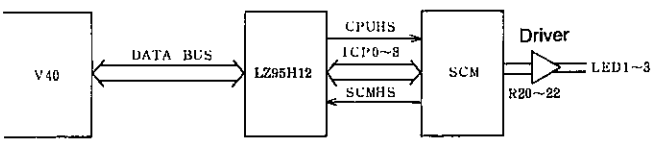
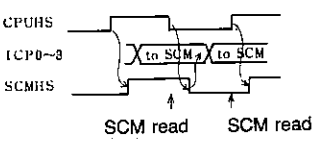


Fig. 3-19 Keyboard LEDs

LED is activated after the SCM receives the command sent from the V40 via the LZ95H12. Communication between the LZ95H12 and the SCM is carried out by handshaking. The data are sent on four bidirectional bus ICP0–3. The signal CPUHS is used from the LZ95H12 for handshake control and SCMHS from the SCM. The figure below shows an example of data transfer.



3-17. LCD control circuit

3-17-1. I/O mapping

The table below shows the I/O address assignment of the MDA and ATT (CGA).

I/O Address	Read/ Write	Bit	Description
77H	R/W	0	ATT (CGA/MDA). 1: ATT (CGA) Mode, 0: MDA Mode
		4	RVVD (Reverse video) 1: Reverse video enable
78H	R/W	4	CURBLK0, 1 (Cursor Blink Rate 0, 1)
		5	0: Steady 1: 1/64 S blink 2: 1/32 S blink 3: 1/16 S blink
		6	ATTBLK0, 1 (Attribute blink Rate 0, 1)
		7	0: Steady 1: 1/64 S blink 2: 1/32 S blink 3: 1/16 S blink
Index Register 3B4H (ATT=0) 3D4H (ATT=1)	W	0	IDX0 (Index Address 0)
		1	IDX1 (Index Address 1)
		2	IDX2 (Index Address 2)
		3	IDX3 (Index Address 3)
		4	IDX4 (Index Address 4)
		5	Not used
		6	Not used
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0AH)	W	0	CSSL0 (Cursor Start Scan Line 0)
		1	CSSL1 (Cursor Start Scan Line 1)
		2	CSSL2 (Cursor Start Scan Line 2)
		3	CSSL3 (Cursor Start Scan Line 3)
		4	CSSL4 (Cursor Start Scan Line 4)
		5	CSSL5 (Cursor Start Scan Line 5)
		6	CSSL6 (Cursor Start Scan Line 6)
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0BH)	W	0	CESL0 (Cursor End Scan Line 0)
		1	CESL1 (Cursor End Scan Line 1)
		2	CESL2 (Cursor End Scan Line 2)
		3	CESL3 (Cursor End Scan Line 3)
		4	CESL4 (Cursor End Scan Line 4)
		5	CESL5 (Cursor End Scan Line 5)
		6	CESL6 (Cursor End Scan Line 6)
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0CH)	W	0	DSA8 (Display Start Address 8)
		1	DSA9 (Display Start Address 9)
		2	DSA10 (Display Start Address 10)
		3	DSA11 (Display Start Address 11)
		4	DSA12 (Display Start Address 12)
		5	DSA13 (Display Start Address 13)
		6	Not used
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0DH)	W	0	DSA0 (Display Start Address 0)
		1	DSA1 (Display Start Address 1)
		2	DSA2 (Display Start Address 2)
		3	DSA3 (Display Start Address 3)
		4	DSA4 (Display Start Address 4)
		5	DSA5 (Display Start Address 5)
		6	DSA6 (Display Start Address 6)
		7	DSA7 (Display Start Address 7)
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0EH)	R/W	0	CSA8 (Cursor Address 8)
		1	CSA9 (Cursor Address 9)
		2	CSA10 (Cursor Address 10)
		3	CSA11 (Cursor Address 11)
		4	CSA12 (Cursor Address 12)
		5	CSA13 (Cursor Address 13)
		6	Not used
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0FH)	R/W	0	CSA0 (Cursor Address 0)
		1	CSA1 (Cursor Address 1)
		2	CSA2 (Cursor Address 2)
		3	CSA3 (Cursor Address 3)
		4	CSA4 (Cursor Address 4)
		5	CSA5 (Cursor Address 5)
		6	CSA6 (Cursor Address 6)
		7	CSA7 (Cursor Address 7)
3B8H (ATT=0)	W	0	Not used
		1	Not used
		2	Not used
		3	0: Video disabled, 1: Video enabled
		4	Not used
		5	MSB of attribute is 0: intensity, 1: blink
		6	Not used
		7	Not used
3D8H (ATT=1)	W	0	0: 40 x 25 Alpha, 1: 80 x 25 Alpha
		1	0: Character Mode, 1: Graphics Mode
		2	Not used
		3	0: Video disabled, 1: Video enabled
		4	Not used
		5	MSB of attribute is 0: intensity, 1: blink
		6	Not used
		7	Not used
3B8H (ATT=0)	R	0	Horizontal sync
		1	Not used (0 read)
		2	Not used (0 read)
		3	Black/white video
		4	Not used (0 read)
		5	Not used (0 read)
		6	Not used (0 read)
		7	Not used (0 read)
3D8H (ATT=1)	R	0	Display enable
		1	Not used (0 read)
		2	Not used (0 read)
		3	Vertical sync
		4	Not used (1 read)
		5	Not used (1 read)
		6	Not used (1 read)
		7	Not used (1 read)
3DEH (ATT=1)	W	0	640 x 200 APA 0: two 16K alpha pages, 1: one 32K alpha page
		1	Not used
		2	Not used
		3	0: Select low page, 1: select high page
		4	Not used
		5	Not used
		6	0: underline disabled, 1: underline enabled
		7	Not used

3-17-2. VRAM mapping

The LCD control circuit has four 256K-bit (64 x 4-bit) DRAM chips which are used for VRAM, character generator table, and system work area. A 4KB area is used as a VRAM (display buffer) in the MDA mode, or 16KB in the CGA mode, or 32KB in the ATT mode. The ATT mode is an expanded version of the CGA mode which supports 640 x 400 APA mode.

The figure next shows the display buffer memory allocation in each mode.

The 4Kbytes monochrome adapter display buffer is mirrored into eight different address 4Kbytes address ranges. The 16Kbytes graphics adapter display buffer is mirrored into two 16Kbytes address ranges.

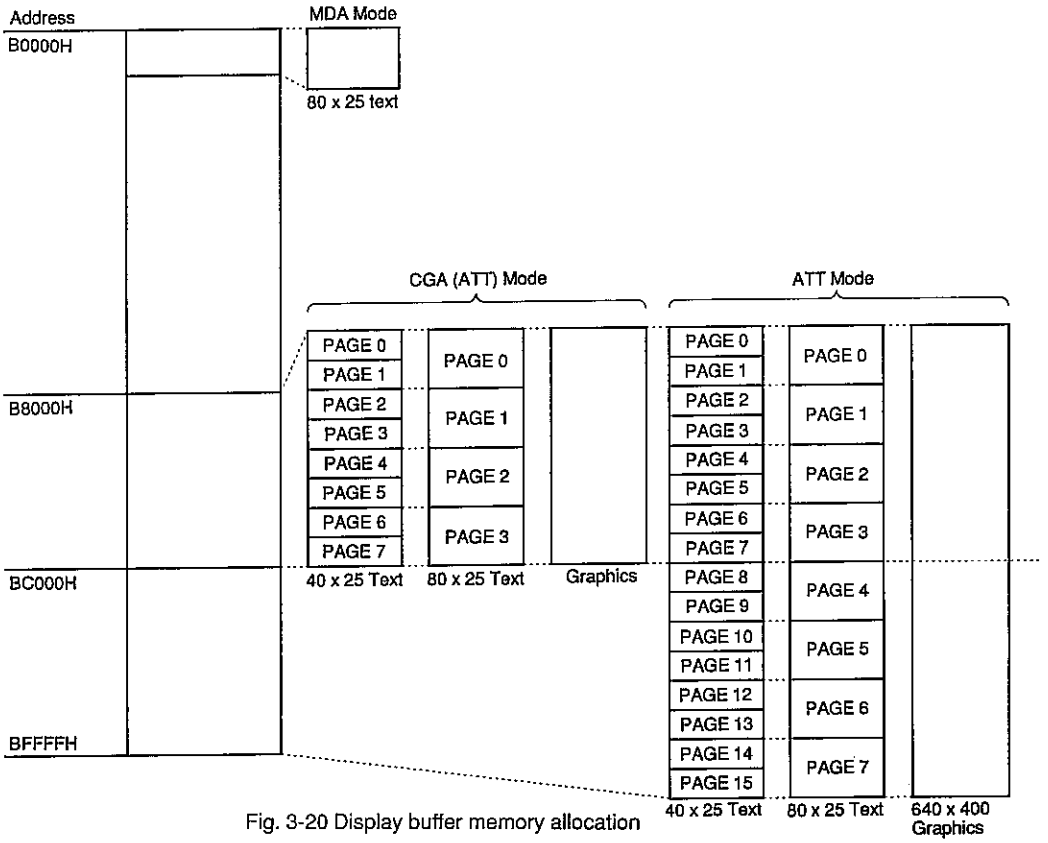


Fig. 3-20 Display buffer memory allocation

3-17-2-1. Text mode

- 80 x 25 text (MDA)
- 80 x 25 text (CGA/ATT)
- 40 x 25 text (CGA/ATT)

The LCD control circuit supports the text 80 x 25 MDA alphanumeric mode and 80 x 25/40 x 25 CGA/ATT alphanumeric mode.

Every character to be displayed has one byte of character code with one byte of attribute. The attribute has four functions described next.

Background			Foreground			Display mode
R	G	B	R	G	B	
0	0	0	0	0	0	Non display
0	0	0	0	0	1	With underline
0	0	1	1	1	1	Normal display
1	1	1	0	0	0	Reverse display

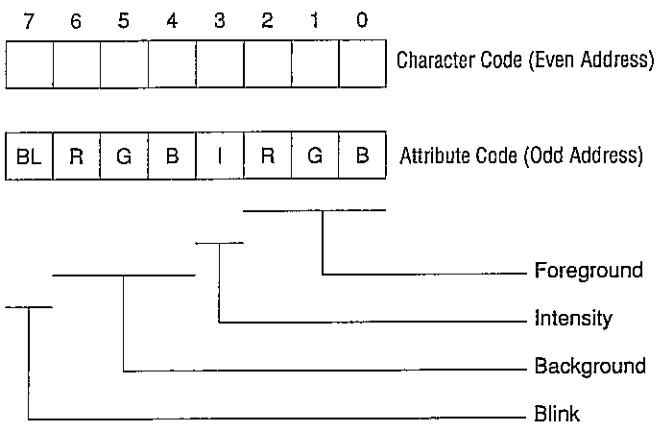


Fig. 3-21 Attribute assignment

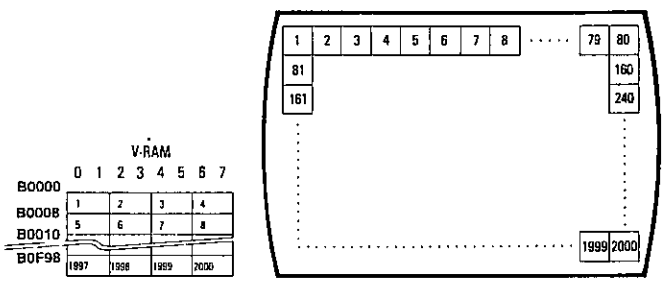


Fig. 3-22 VRAM map in the 80 x 25 text mode (MDA)

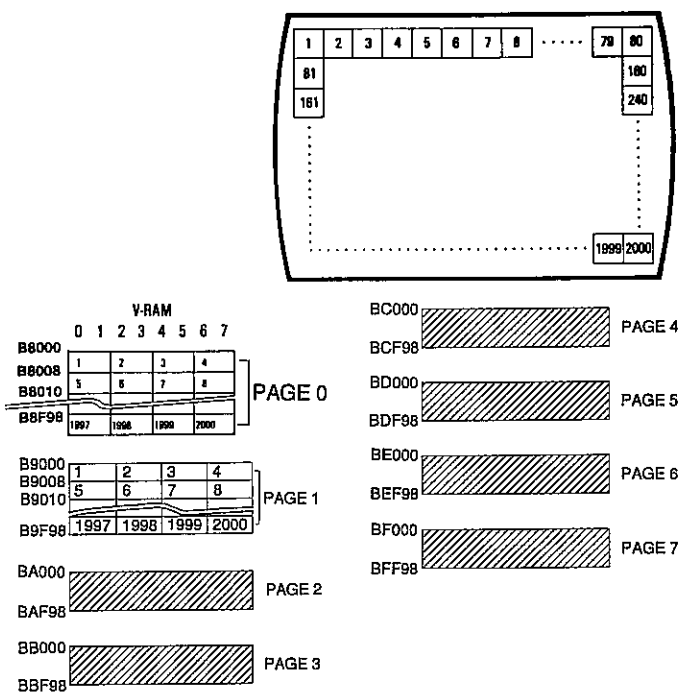


Fig. 3-23 V-RAM map in the 80 x 25 text mode (ATT)

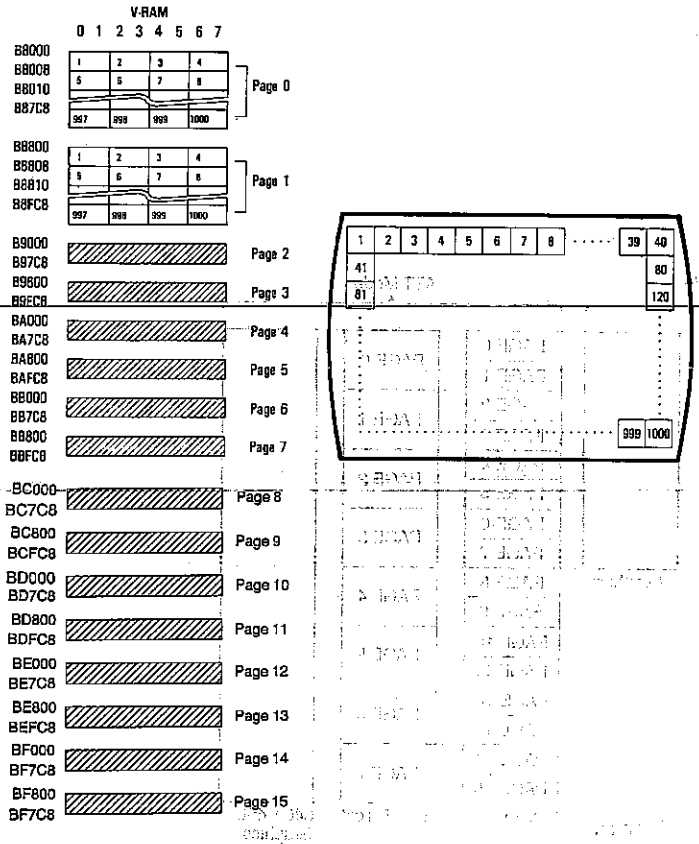


Fig. 3-24 V-RAM map in the 40 x 25 text mode (ATT)

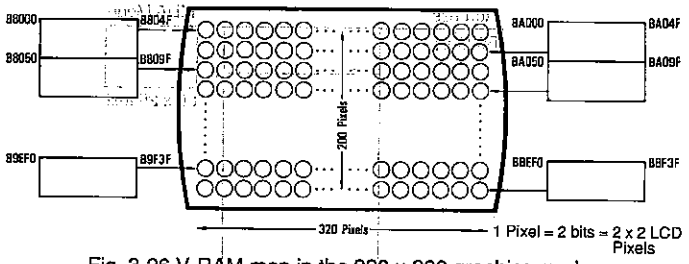


Fig. 3-26 V-RAM map in the 320 x 200 graphics mode

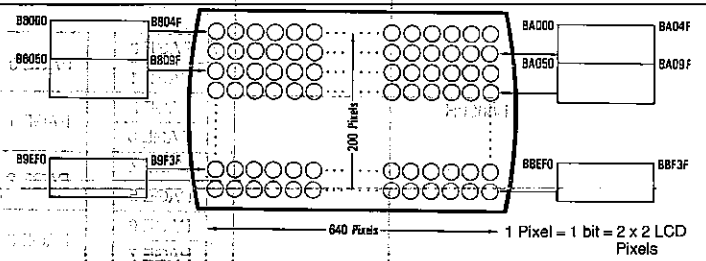


Fig. 3-27 V-RAM map in the 640 x 200 graphics mode

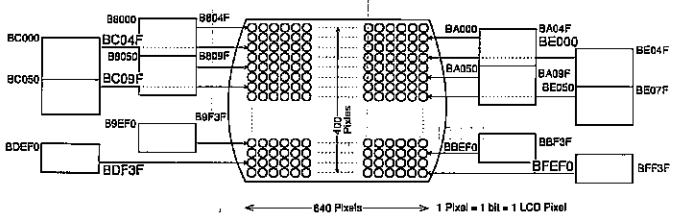
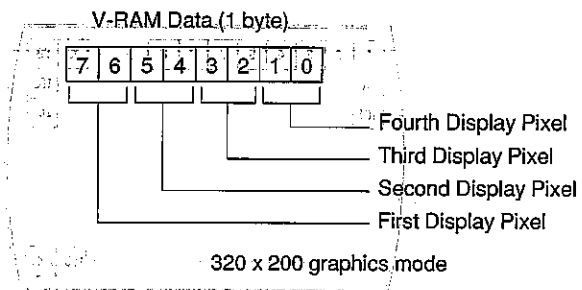


Fig. 3-28 V-RAM map in the 640 x 400 graphics mode

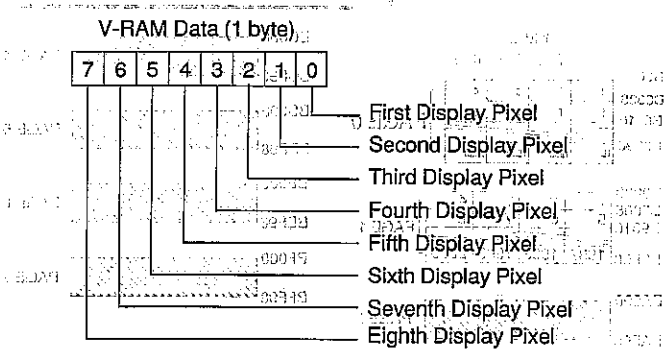
3-17-2-2. Graphics mode

- 320 x 200 graphics (ATT)
- 640 x 200 graphics (ATT)
- 640 x 400 graphics (ATT)

The LCD circuit supports the 320 x 200 graphics mode, 640 x 200 graphics mode, and 640 x 400 graphic mode.
And this circuit uses black for the foreground color and white for the background color in both 640 x 200 and 640 x 400 graphics modes. Each pixel in the 320 x 200 graphics mode is presented by a 2 x 2 block of LCD screen pixels.



320 x 200 graphics mode



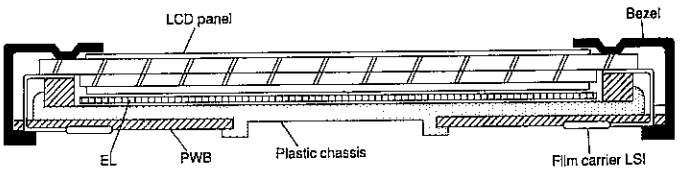
640 x 200, 640 x 400 graphics mode

Fig. 3-25 Bit assignment

CHAPTER 4. LCD UNIT

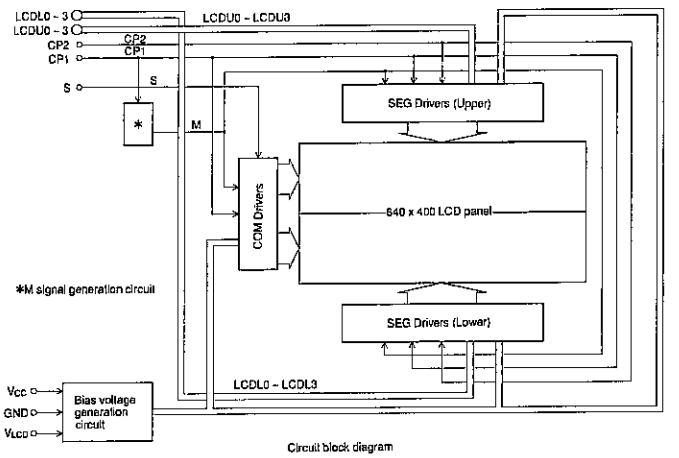
4-1. Structure

A 640 x 400 full dot graphics display unit is employed for the LCD unit which consists of a printed circuit board that contains the LCD panel and its electronic circuits, an electrically connected film carrier LSI chip, and a mechanically held plastic chassis, and a bezel.



4-2. Operational theory

Circuit block diagram and interface signals are shown in the figure next.



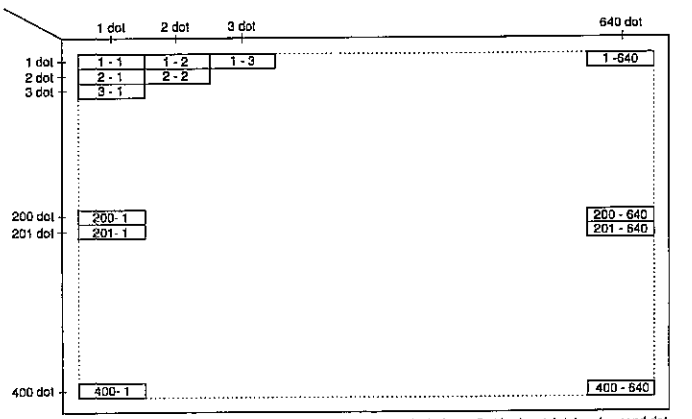
Circuit block diagram

Interface signals

Pin NO.	Symbol	Description	Active signal level
1	S	Scan start signal	"H"
2	CP1	Input data latch signal	H → L
3	CP2	Data input clock signal	H → L
4	Vcc	Logic circuit power supply (+5V)	—
5	GND	Ground	—
6	VLCD	Liquid crystal drive power (–)	—
7	LCDU0	Display data signal (upper half)	H(ON), L(OFF)
8	LCDU1	〃	〃
9	LCDU2	〃	〃
10	LCDU3	〃	〃
11	LCDL0	Display data signal (lower half)	H(ON), L(OFF)
12	LCDL1	〃	〃
13	LCDL2	〃	〃
14	LCDL3	〃	〃

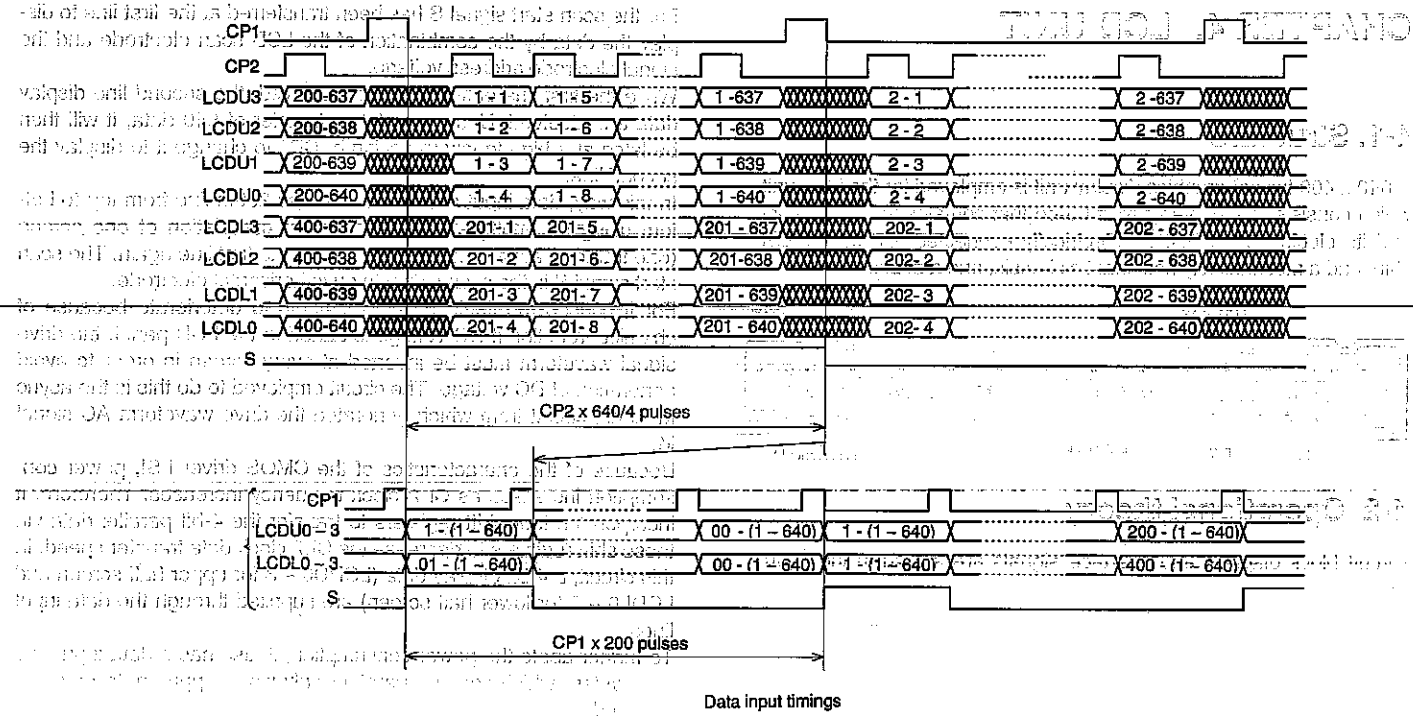
The display screen of this unit is configured of 640 x 400 dots two screens, each screen driven with 1/200 duty.
An 80-pin LSI is used for the LCD driver that consists of a shift register, latch, and LCD drive circuit.
Data are inputted for each line (640 dots) of the screen. From the left side of the screen, 4-bit parallel data are sent one at a time via the shift register with the clock pulse CP2. When the 640 dots data have been received for one display line, the data are latched as a parallel data with respect to the 640 signal electrodes at a high to low transition of the latch signal CP1 to send the drive signal by the drive circuit to the corresponding electrodes.

For the scan start signal S has been transferred at the first line to display the data by the combination of the LCD scan electrode and the signal electrode address voltage.
While the first line data are being displayed, the second line display data are received. Upon completing transfer of 640 data, it will then be latch at a high to low transition of CP1 to change it to display the second line.
In this way, data input are repeated to the 200th line from top to bottom using the multiplexed method. After completion of one screen (one frame), data are then received from the first line again. The scan start signal S is the scan signal to drive horizontal electrode.
For it causes the liquid crystal elements to deteriorate because of chemical reaction if DC voltage is added to the LCD panel, the drive signal waveform must be inverted at every screen in order to avoid generation of DC voltage. The circuit employed to do this is the async M signal circuit from which generated the drive waveform AC signal M.
Because of the characteristics of the CMOS driver LSI, power consumption increases as CP2 clock frequency increases. Therefore, it incorporates four shift registers to transfer the 4-bit parallel data via these shift registers to decrease the CP2 clock data transfer speed. In this circuit, a 4-bit display data (LCDU0 ~ 3 for upper half screen and LCDL0 ~ 3 for lower half screen) are supplied through the data input lines.
To further abate the power consumption, it also has a data input bus line system which comes operating only when appropriate data are received.
The following shows the screens signal electrode data inputs vs. driver LSI chip select signal.
The driver LSI of the left end screen is first elected. When the 80-dot data (20CP2) has been supplied, the driver LSI adjacent to right is then selected. This continues until the data are sent to the driver LSI at the screen right.
This process occurs simultaneously for signal electrode signal LSIs of both screens. In this manner, data of both screens are supplied via 4-bit bus line starting from the left end of the screen.
For the graphics display unit does not contain the refresh RAM, it becomes necessary to input the data and timing pulse when the screen is still.
The following shows the dot table of the display, data input timing chart, and input signal timing.

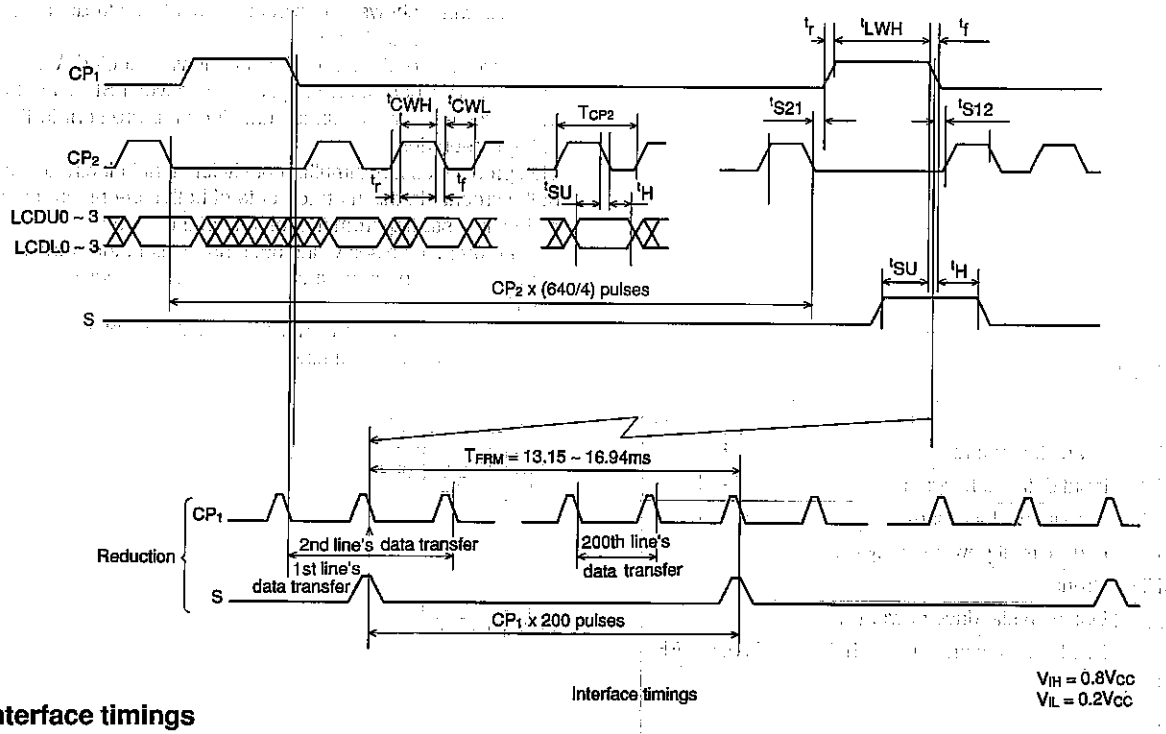


NOTE: 1 and 2 indicate first horizontal dot and second dot.

Display dot chart



Data input timings



Interface timings

$V_{IH} = 0.8V_{CC}$
$V_{IL} = 0.2V_{CC}$

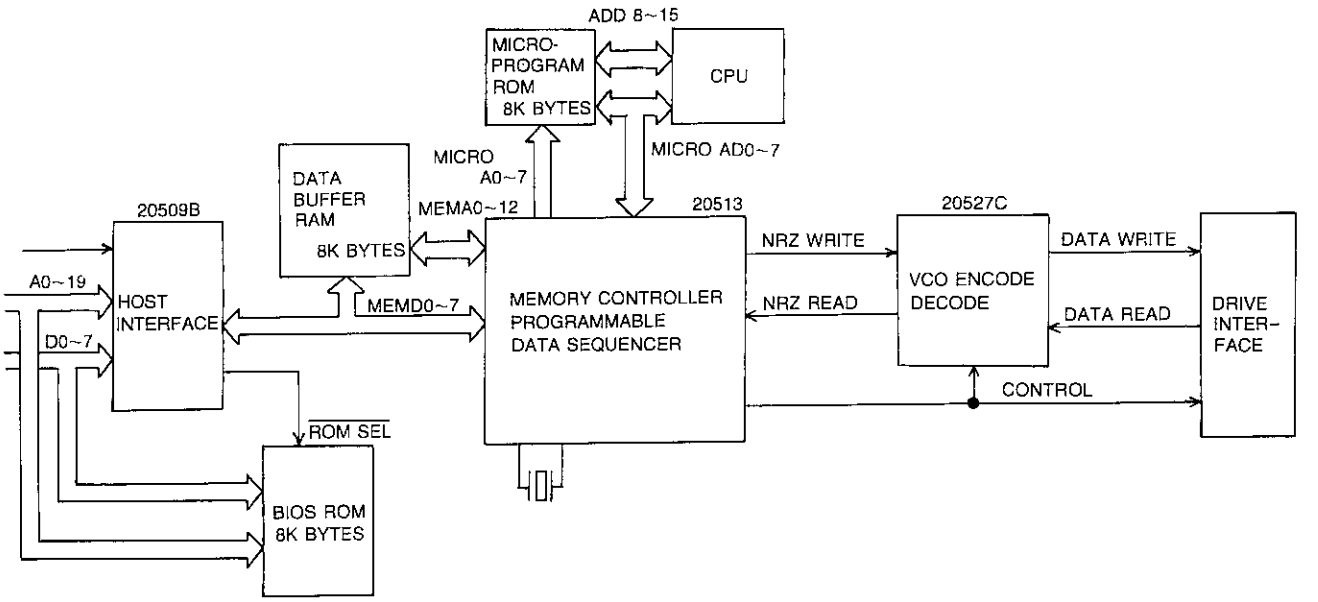
Rated interface timings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Frame cycle	T_{FRM}	13.15		16.94	ms
Clock cycle	T_{CP2}	342			ns
"H" level clock width	t_{CWH}	145			ns
"L" level clock width	t_{CWL}	145			ns
"H" level latch clock width	t_{LWH}	130			ns
Data setup time	t_{SU}	100			ns
Data hold time	t_H	100			ns
Clock allowable time from CP2 ↓ to CP1 ↑	t_{S21}	0			ns
Clock allowable time from CP1 ↓ to CP2 ↑	t_{S12}	0			ns
Clock rise and fall time	tr, tf			50	ns

CHAPTER 5. HARD DISK INTERFACE & HARD DISK DRIVE

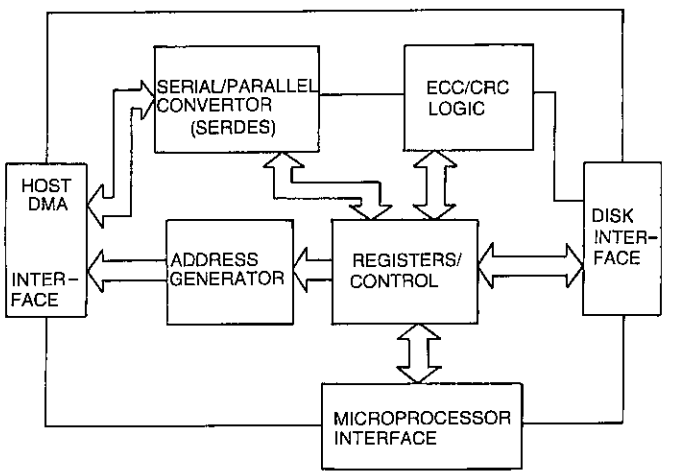
1. HARD DISK INTERFACE

1-1. Block diagram



1-2. Host Inteface (20509B)

The ECC/CRC block generates and checks the ECC or CRC bytes that are appended to the disk-sector ID and data fields.
When the floppy format is selected, both ID and Data fields will use the serial implemented polynomial.
Four CRC and ECC polynomials are available depending on the setting of internal register's bit.
The Host/Buffer Interface consists of an 8-bit data bus a 13-bit address bus addressifng up to 8K bytes external RAM and various control signals.
The Microprocessor Interface consists of an 8-bit multiplexed address/data bus, and 8-bit demultiplexed address bus and various microprocessor bus control signals.
The Drive Interface contains the serial data lines to and from the disk (or encode/decode circuitry) and various control signals needed during reading and writing.



BLOCK DIAGRAM

1-3. Memory controllor/programmable data sequencer (20531)

The figure above illustrates a conceptual block diagram of the Memory Controller/Programmable Data Sequencer. It includes the main internal logic blocks and the interface blocks. Each of these is described below.
The Registers/Control block contains 2 groups of 8-bit internal control registers and associated control logic.
One group of registers is used for the Memory Controller section of the chip, the other group is used for the Programmable Data Sequencer section. Some of these registers may be individually written to by the microprocessor to initialize the parameters that control data transfer, and to initiate the data transfer command. The other registers may be individually read by the microprocessor to obtain status information about command execution.
The Address Generator block outputs addresses to the RAM buffer memory during the transfer of data between buffer & host, and between buffer and disk. The Address Generator automatically increments the address value to point to the next location in the buffer after each byte of data has been transferred.
The Serial/Parallel Data Converter block translates between the serial NrZ form of data used to and from the disk drive, and the byte-parallel form used on the host memory bus. High speed shift registers are used to perform the conversion.

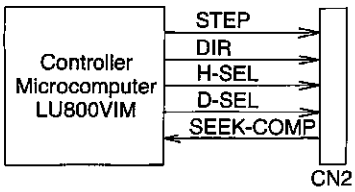
1-4. RLL modulation and demodulation (20527)

The RLL modulator/demodulator modulates the NRZ serial data into 2-7 code serial data transferred from the 20513, to create data to be written on the disk.
On the contrary, the 2-7 code read from the disk are demodulated in to the NRZ serial data to be transferred to the 20513.
20527 includes VCO to select data demodulation VFO control and clock.
Shown below is the table for the NRZ and 2-7 code conversion.

NRZ DATA	2-7 CODE
01	0100
00	1000
111	000100
100	001000
101	100100
1101	00100100
1100	00001000

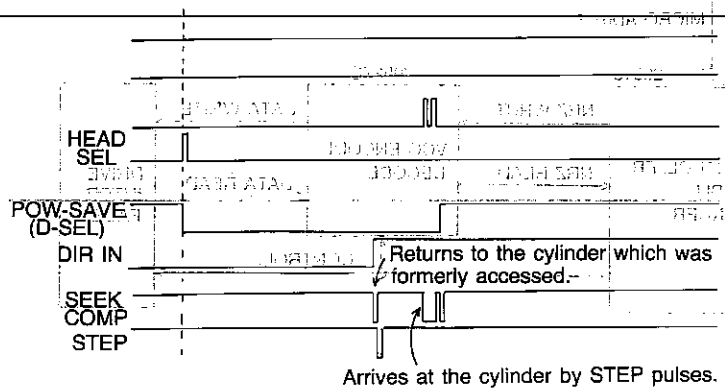
TABLE

1-5. SEEK operation

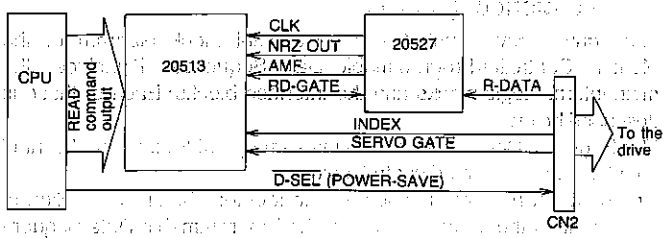


When D-SEL becomes low with the head locating in the shipping zone, the drive returns to the cylinder which was formerly accessed. When the process is completed, the SEEK-COMP is made low. The microcomputer confirms this signal to set DIR IN for instructing the moving direction of the head. After setting DIR IN, STEP pulses are applied in accordance to the movement of the cyclinder. When the SEEK COMP becomes low, the SEEK operation of the cylinder is completed.

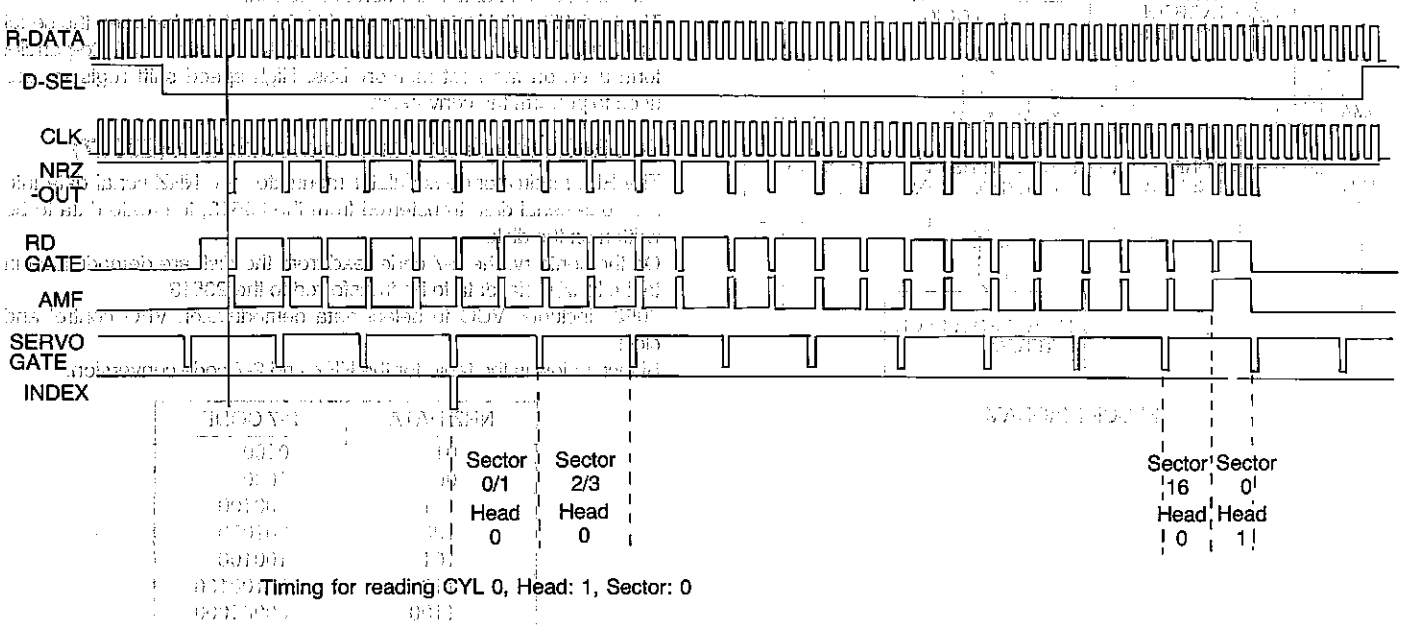
(Note) The HEAD SEL which selects HEAD 0 or 1 is specified almost simultaneously with the D-SEL.



1-6. READ operation

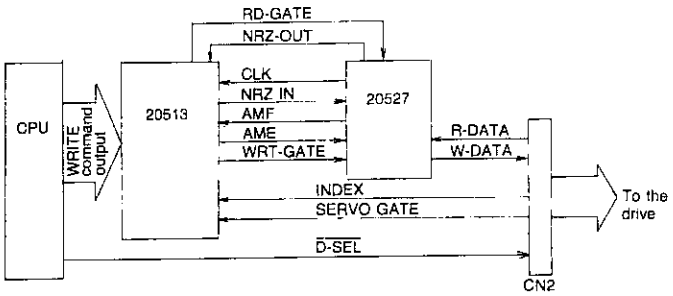


- After seeking the cylinder when S-SEL becomes low, the RD-GATE becomes high and the serial data from NRZ OUT are converted into 8-bit data. This operation is repeated until the target sector is found. When the target sector is found, 512-byte data is input to make D-SEL high, completing READ operation.
- R-DATA : Written data are output in the 2-7 system from the drive.
- DF-SEL : Signal to access the drive.
- CLK NRZ-OUT : Data output obtained by converting 2-7 data into binary codes. (Supplied at CLK rising edge.)
- RD-GATE : Validates CLK/NRZ-OUT data.
- AMF : Becomes high when detecting 8T missing pulse, and becomes low at RD-GATE falling edge.
- SERVO GATE : 17 units are provided for one cylinder, and 2 sectors for 1 pulse.
- INDEX : Indicates the head of the cylinder.

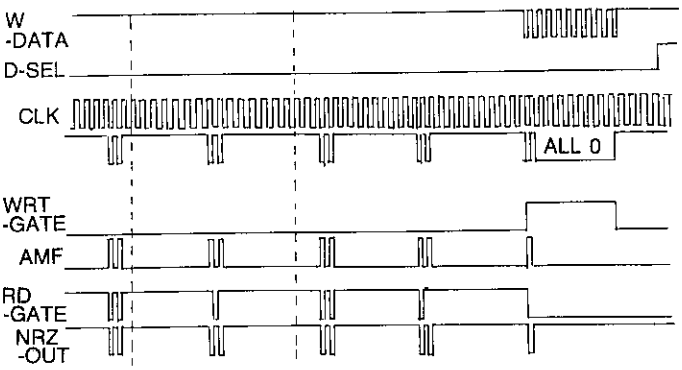


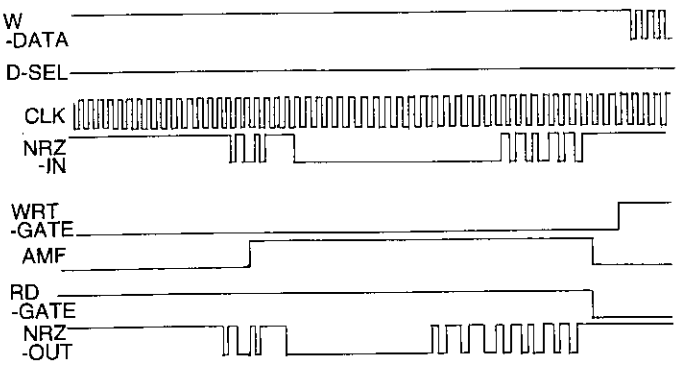
Timing for reading CYL 0, Head: 1, Sector: 0

1-7. WRITE operation



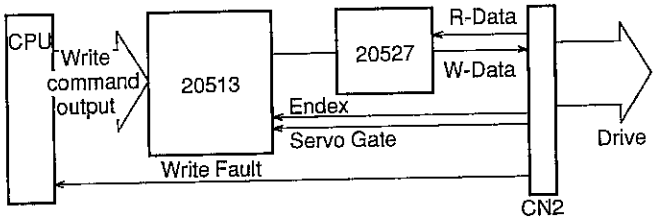
- When the target cylinder and sector are found by READ operation, WRT-GATE become high to write data.
- CLK : Binary data are synchronized with CLK falling edge
  NRZ-IN to provide 20527 input.
- WRT-GATE: Validates data supplied from NRZ-IN.

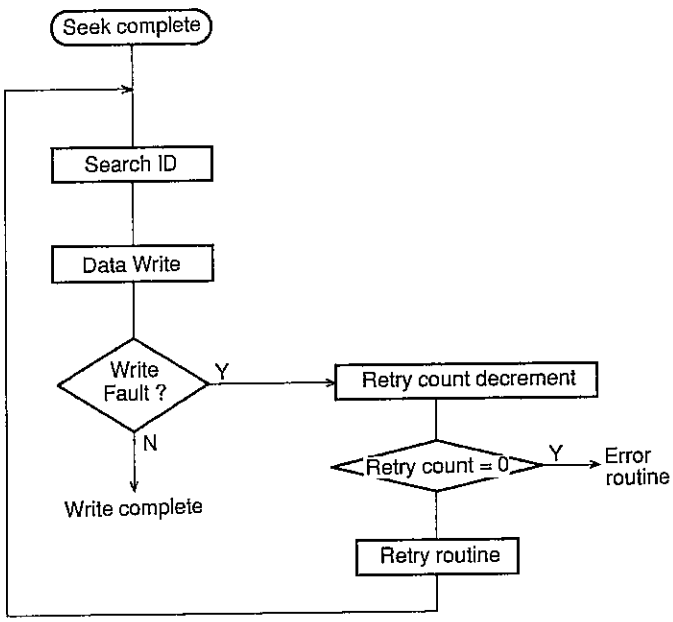




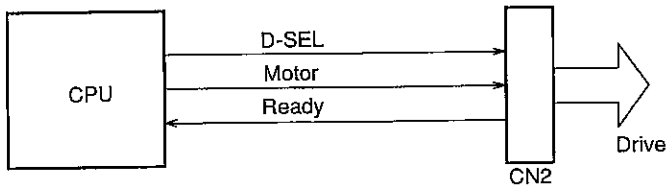
1-8. Write retry

With the JD-3848H0S0 40M hard disk, a write fault is asserted immediately after the servo gate signal against vibration and impact received during write. On the other hand, the controller makes a maximum eight retrials against a write fault.





1-9. Motor on/off command



(1) Fig.1 shows the motor on/off sequence.

Motor startup timing is discussed next.

① When the motor is at halt, a maximum 10 seconds are required before the drive becomes ready; the time before the motor on command completion status is received after the motor on command was issued.

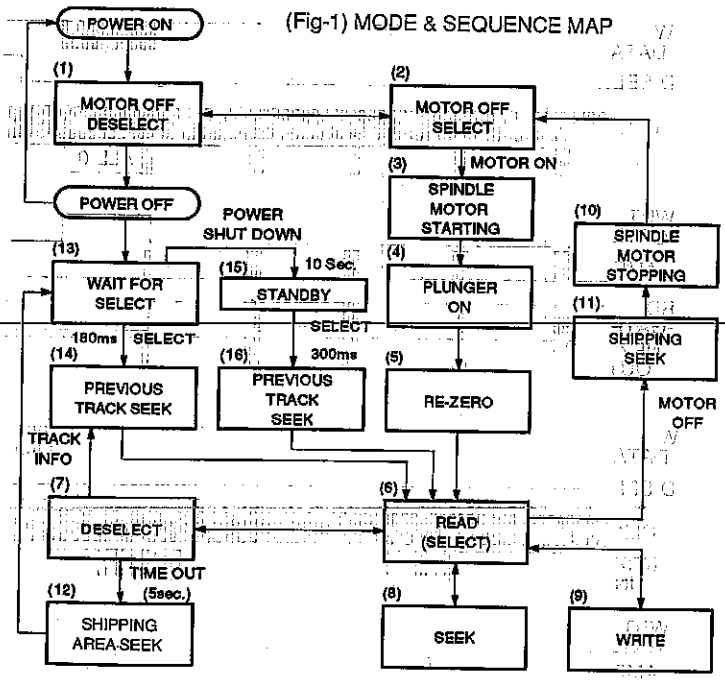
② If the motor off command was issued continuously along with the motor on command while the motor is running, a maximum 15 seconds are required before the motor on completion status is obtained after the motor on command was issued.

(2) Motor auto-off timer

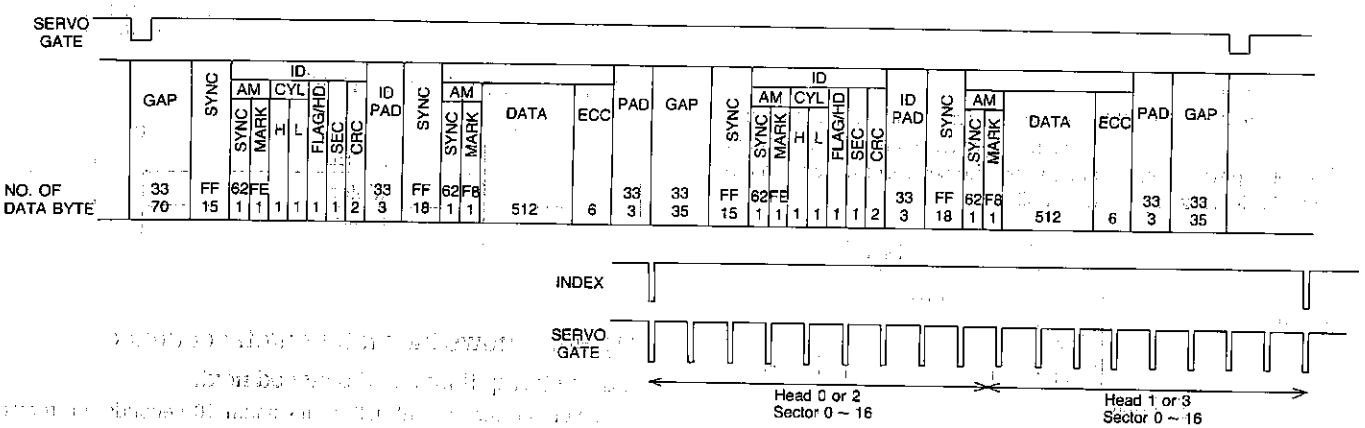
① The auto-off timer can be programmed from 5 to 2 minutes 15 seconds (01~FF hex) in an increment of 5 seconds. When "00" is given, the timer is set infinitive, that is, the auto-off mode turns invalid.

② When a command that deselects the drive such as read and write is issued, the auto-off times is started to decrement upon the time the deselect is commanded.

(Fig-1) MODE & SEQUENCE MAP



1-10. Formatting chart



(Note) Formatting at inter-leave 1.

2. HARD DISK DRIVE

2-1. Hard disk drive unit specifications

2-1-1. Parts number of the drive

JD3848H00

2-1-2. Disks

Disks	2
Cylinders	615+1 (spare)
Total tracks	2460+2 (spare)

2-1-3. Head

Physical	4 heads
Logical	8 heads

2-1-4. Maximum storage capacity

Unformatted	53.26M bytes
Formatted	42.89M bytes

2-1-5. Recording method

Method	2-7 RLL
Data transfer speed	7.5M bits/sec
Recording density	25610 BPI
Recording density	17073 FCPI
Track density	941 TPI

2-1-6. Spindle motor

Revolutions	2592.6 rpm
Mean wait time	11.57 msec
Startup time	10 sec, max.

2-1-7. Format

(Physical sectors/physical	tracks)	17
Formatted sectors/physical	tracks	34
Formatted sector size		512 bytes

2-1-8. Access time (average at 25°C, rated voltage including settling time)

18 ms, track to track
45 ms, average
75 ms, full stroke

2-1-9. Operating environments

Operating temperature (small temperature controlled chamber)

0~50°C (55°C maximum at the top plate of the drive), or 65°C maximum subject to test conditions given in separate page.

Non-operating temperature

–20~60°C

Storage condition (packaged)
-20~60°C, within 1,000 hrs

Cycle storage (packaged)
Within 1 hour, 5 cycles at limited temperatures

Temperature slope
15°C/H maximum when operating or 20°C/H maximum when not operating

Operating humidity
20~80%RH (wet ball at 29°C, maximum), without moisture condensation

Non-operating humidity
10~80%RH (wet ball at 29°C, maximum), without moisture condensation

Environmental air
Must be free from corrosive gas and salt.

Noise
40dB maximum during standby (A), slow
50dB maximum during seek (A) slow

NOTE: Measuring direction 1 meter above the drive unit
Measuring conditions Room temperature, room humidity, rated voltage

2-1-10. Reliability

MTBF	20,000 hrs
MTTR	30 minutes
P.M.	None
Life	5 years
CSS	20,000 start/stop
Media defects	27 maximum excluding the cylinder 0
Defect size	11 bits maximum
Error rate	
Soft error (NOTE)	10^{-10} maximum
Hard error	10^{-12} maximum
Seek error	10^{-6} maximum

NOTES: (1) Recoverable after 4 retries for a soft error.
(2) Unrecoverable after 4 retries for a hard error.
(3) Above retrial errors are on the same cylinder without including recal.

2-1-11. Shock resistance

Operating

During write	5G, 10 ms (all axial directions) (half sinusoidal waveform) (without hard error)
During read	5G, 10 MS 10 ms (all axial directions) (half sinusoidal waveform) (without hard error)
Non-operating	70G, 10 ms (all axial directions) (half sinusoidal waveform)

2-1-12. Vibration resistance

Operating	5~10Hz, 1.0mm, full amplitude 10~500Hz, 0.2G, peak
Non-operating (all directions)	5~10Hz, constant deviation, 10.16 mm 10~500hZ, 2.0G, peak
Sweep speed	1 Oct./minute

2-1-13. Altitude

Operating	0~2400 meters
Non-operating	0~7600 meters

2-1-14. Weight

(Shield cover inclusive) 790 grams, typical

2-1-15. Physical dimensions

Attachment-1

2-1-16. DC power (HDD only)

	Allowable error	Allowable ripple	Consumption current (max.)
+12V	±0.6V	100mVp-p	150mA (200mSec.)
+5V (MOTOR)	±0.5V	200mVp-p	1,300mA
+5V (LOGIC)	±0.25V	100mVp-p	150mA

* Ripples are sinusoidal waveform of 20Hz to 120Hz and white noise of 10Hz to 1MHz.

* Ripple is included in the allowable error.

2-1-17. Power consumption (25°C ±2°C, rated voltage)

		(Maximum)
Motor on:	Read	2.5W
	Wrote	2.8W
	Seek	5.1W (7.7W, peak)
	Waiting	1.9W
	Standby	1.2W
Motor starting (5 seconds, maximum)		7.9W Peak

1-18. Format

(1) Physical format
Cylinders 0 to 614 are physically formatted.
For the hard sectors, hard track format is done for each physical head.
(Cylinder 0 is not included)

(2) Sector interleave 1 (See attached drawing, Sector interleave)

NOTES:
- The format is done according to JD-C3848H0S0 controller board.
- The cylinder 615 (spare cylinder) is for use of the vendor only.
- Cylinders 0, 1, 2, and 3 are for defect free cylinders.

2-1-19. Connector specification

The following connector or its equivalent will be used.
Drive side" D50226-B002JL (Sumitomo 3M), black
Compatible connector: 50126-B000EL (Sumitomo 3M), strain relief, 3448-50126

2-1-20. Hard disk drive interface specification

PIN	I/O	SIGNAL	PIN	I/O	SIGNAL
1		GND	2	O	R. DATA
3		GND	4	I	W. DATA
5		GND	6	I	HEAD SELECT 1
7	I	POWER SAVE	8	O	(SHIP READY)
9		GND	10	I	READ/WRITE
11	I	MOTOR ON	12	I	HEAD SELECT 0
13	I	DIRECTION IN	14	I	STEP
15	O	WRITE FAULT	16	O	SEEK COMPLETE
17	O	SERVO GATE	18	O	INDEX
19	O	TRACK 000	20	O	READY
21		GND (LOGIC)	22		+5V (LOGIC)
23		GND (MOTOR)	24		+5V (MOTOR)
25		GND	26		+12V

NOTE-1: See the list below for the logic of pin 6 head select 1 and pin 12 head select 0.

	HEAD SELECT 0	HEAD SELECT 1
HEAD 0	"H"	"H"
HEAD 1	"L"	"H"
HEAD 2	"H"	"L"
HEAD 3	"L"	"L"

NOTE-2: The pin 6 is not connected because it is used for the factory only.

NOTE-3: Output on the pin 8 goes low when the head moved over the shipping position which can drive the red LED. Becomes valid when READY become low.

NOTE-4: I/O except for the pin 8 are 74HC compatible (2K pullup attached for input)

2-1-21. Drive margin

± 9 nsec or above

Measuring condition: 50°C without moisture within a small temperature controlled chamber, rated voltage.
Has random pattern and write compensation.

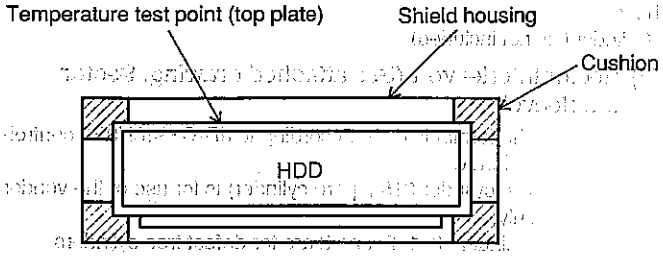
2-1-21. Installing direction

The hard drive should normally be installed horizontal (label facing up) or transverse (label and connector facing side). Need discussion if to be installed with tilt.
Never install it with the connector facing up or down.

HDD temperature and moisture assurance test conditions

(1) Temperature and moisture assurance limits

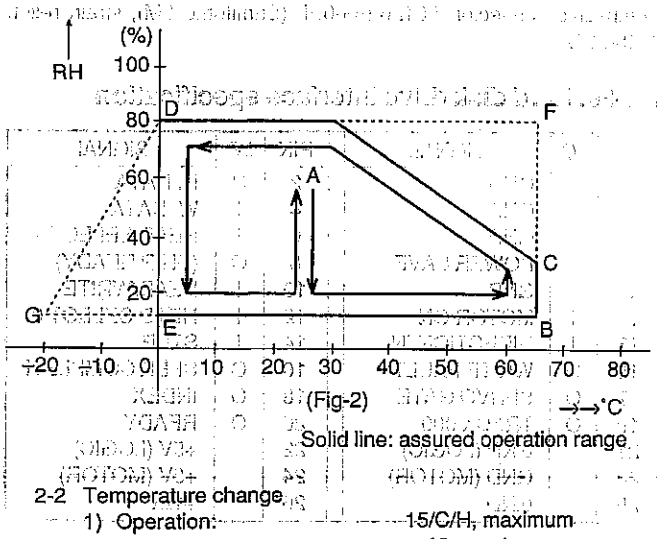
1-1 Operation 0°C~65°C (10%~80%RH, non-condensing)
(2) According to the temperature test conditions.



(Fig-1)

(2) Humidity test condition

2-1



(Fig-2)

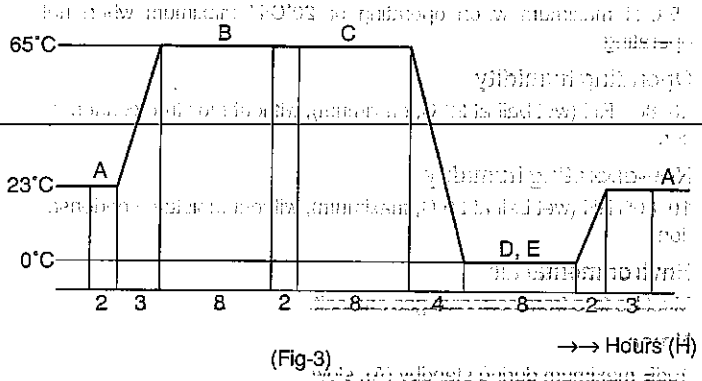
Solid line: assured operation range

2-2 Temperature change

1) Operation: 15/C/H, maximum
2) Storage: 20°C, maximum
3) Maximum wet ball humidity: 29°C

(3) Operating test method

3-1 Humidity can be any under 0°C.
3-2 The test will take place in the order of temperature change, starting from the room temperature of 23°C (arrowhead)
3-3 Cyclic temperature and humidity operating test (temperature at the top plate as shown in Fig.1)



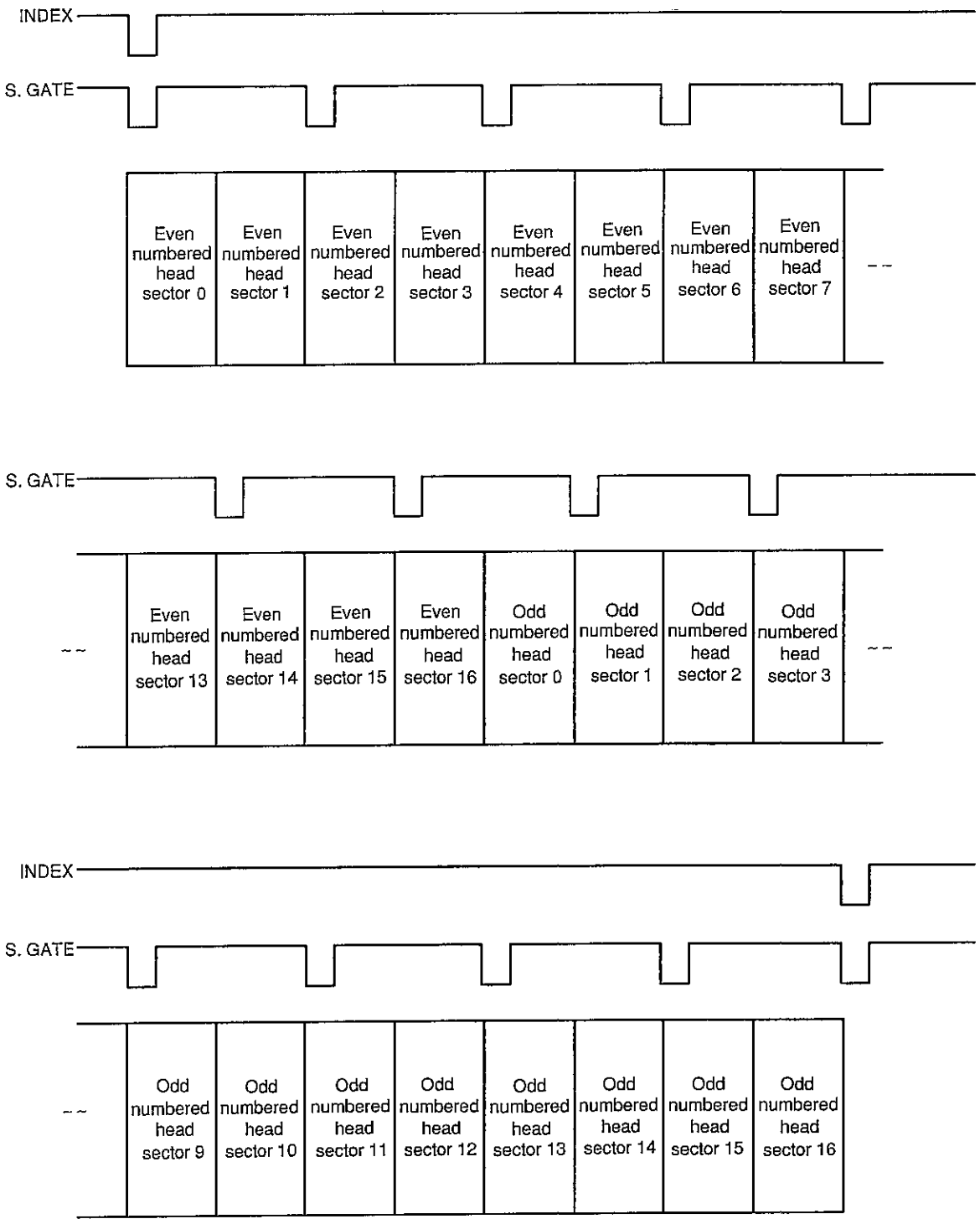
(Fig-3)

3-4 The above temperature/humidity test comprises a cycle.

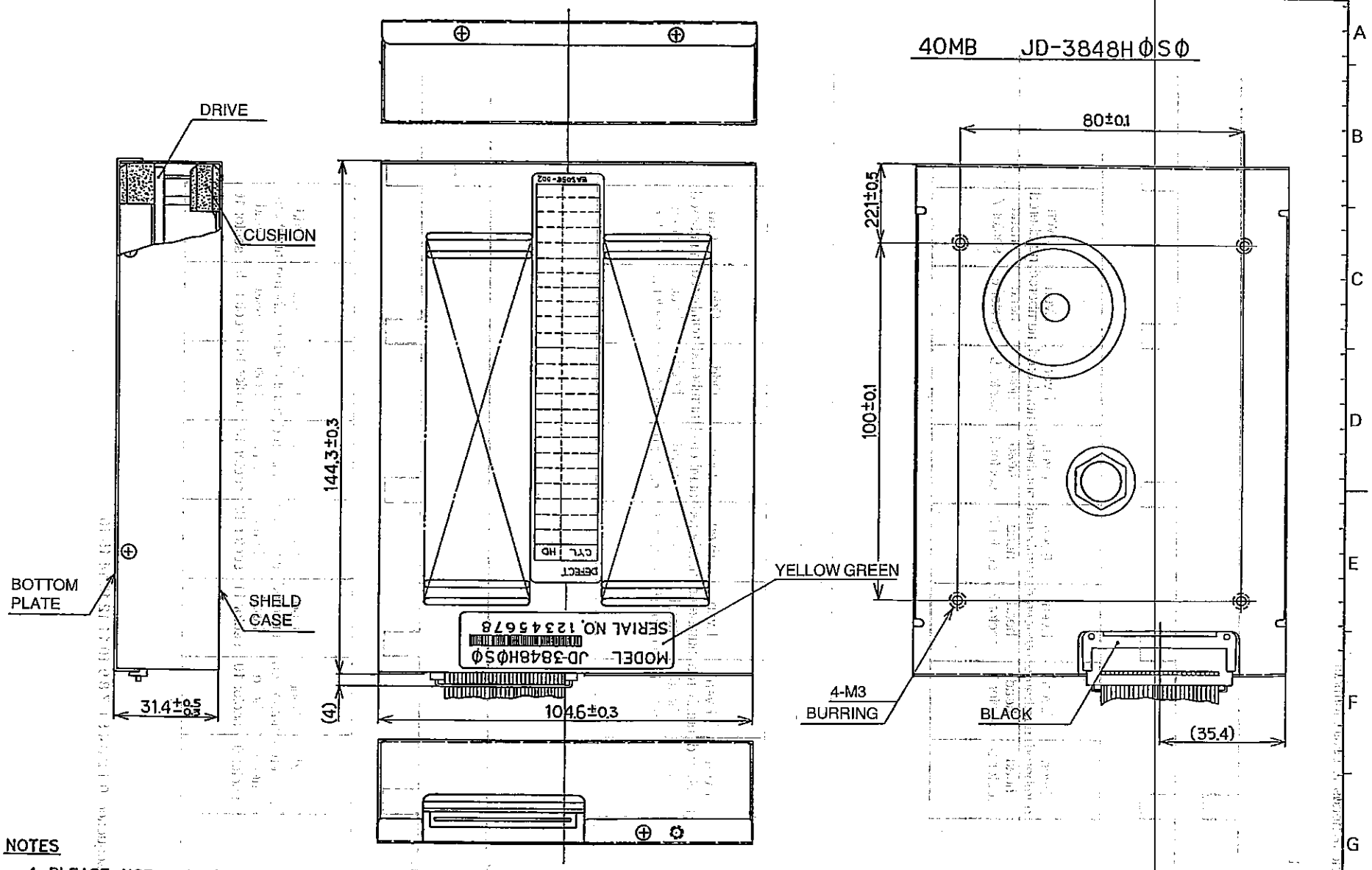
ATTACHMENT

Sector interleave table (8 heads/17 sector formats)

Interleave factor 1



Sector sequence: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16



NOTES

1. PLEASE USE 4-M3 (HOLES FOR SCREW) TO MOUNT TO BRACKET.
2. MOUNTING SCREW (4-M3) MAY NOT JUT MORE THAN 3mm FROM THE BOTTOM OF DRIVE SHIELD CASE.

CHAPTER 6. POWER SUPPLY CIRCUIT

6-1. Block diagram

Fig. 6-1 shows the block diagram.

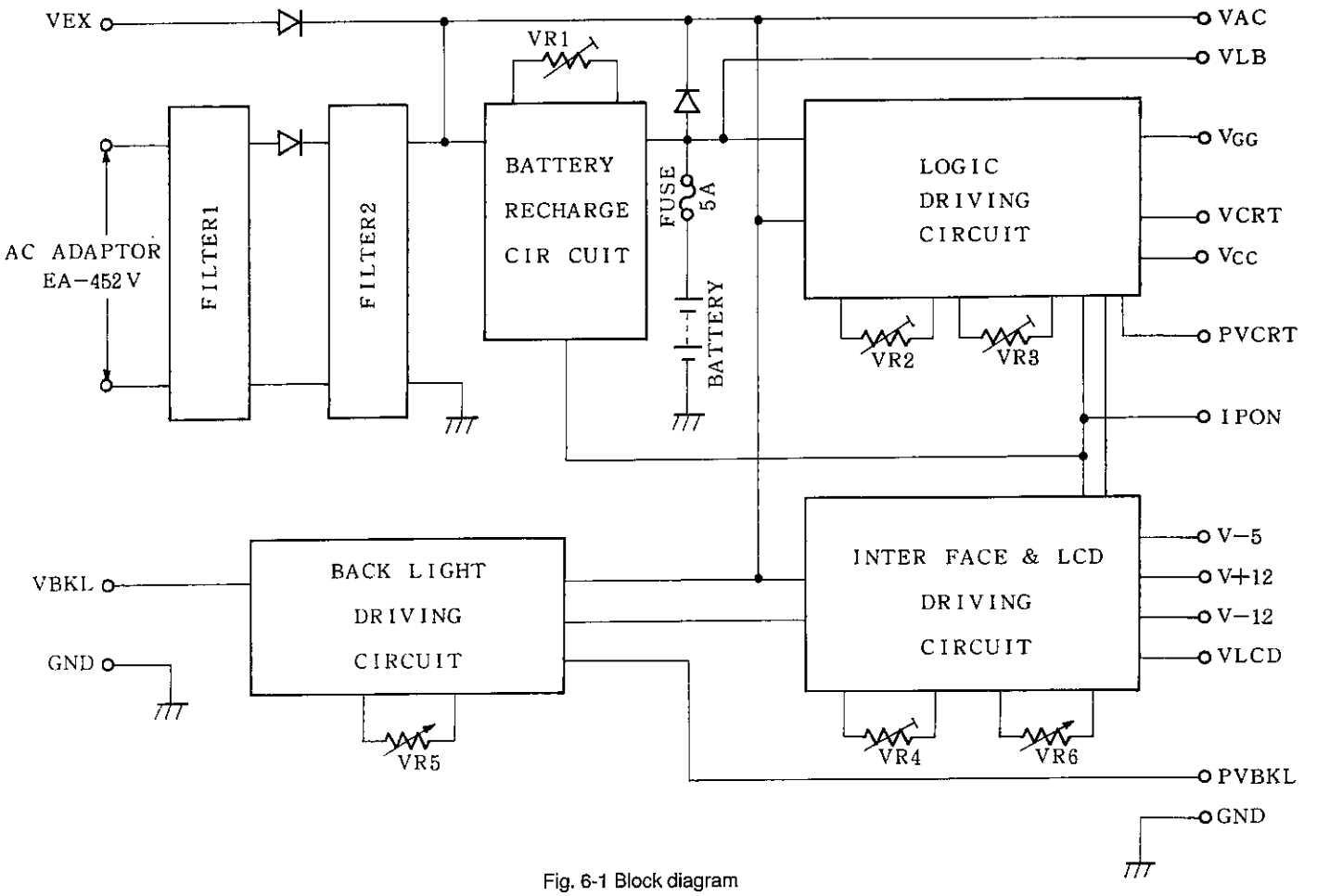


Fig. 6-1 Block diagram

6-2. Electric characteristics

(1) Input voltage

This power supply unit could be operated by using one of the following input voltage and the combination of them.

a. AC adaptor (CE-452V) 9.0V±0.5V 2.5A
b. Lead battery (UBATZ1003ACZZ) 5.0V–6.5V 4.2Ah
c. External input 9.0V±0.5V 2.5A

(2) Non-load current

Table 6-2 shows the input current from the battery connector when all outputs are non-load with 6.3V input from battery connector without using AC adaptor.

IPON	CURRENT
Low	less than 500μA
High	less than 200mA

Table 6-1

(3) Monitering output

The power supply unit outputs the following 2 monitering outputs.

a. VLB

The VLB tells the battery voltage to the system.
The output connect the battery terminal through the diode equal of RK13.

b. VAC

The VAC tells whether the AC adaptor is connected or not.
The output should be more than 6.5V while the AC adaptor is connected.

(4) Battery voltage detection

When VLB voltage is changed according to the value in table 6-2 without connecting AC adaptor, the VGG output voltage satisfies the value in the table 2.
(IPON is set to low. VGG load is adjusted to 1mA.)

VLB voltage (V)	VGG voltage (V)
from 0 to 4.0	less than 0.3
from 0 to 5.1	4.75 – 5.25
from 6.0 to 4.8	4.75 – 5.25
from 6.0 to 4.0	less than 0.3

Table 6-2

(5) Output voltage

The power supply unit could supply the following outputs by either the inputs of AC adaptor, battery, or external input.
The converting efficiency should be more than 70% when using the battery as the input.

a. VGG (+5V±0.25V)

The VGG output is always supplied to the logic ICs on the Main PCB.

b. VCC (+5V±0.25V)

The VCC output is supplied to the logic ICs on the Main PCB, LCD unit, FDD unit, and HDD unit while the control signal IPON is high.

c. V+12 (+12V±0.6V)

The V+12 output is supplied to the ICs, the HDD unit and fan while the IPON is high.

d. V–12 (–12V±1.0V)

The V–12 output is supplied to the ICs while the IPON is high.

e. V–5 (–5V±0.25V)

The V–5 output is supplied to the optional MODEM unit while the IPON is high.

f. VLCD (–11.5V ~ –20.7V)

The VLCD output is supplied to the LCD unit while the IPON is high. The output could be changed by the volume to adjust the contlast of the LCD.
The output shouldn't be beyond –26.0V.

g. VCRT (+5V±0.25V)

The VCRT output is supplied to the optional CRT adaptor while the control signals IPON and PVCRT are high.

h. VBKL (AC 35V ~ 100V)

The VBKL output is supplied to the EL pannel while the control signals IPON and PVBKL are high.
The output could be changed by the volume to adjust the brightness of the backlight.
The maximum brightness of the EL panel should be 80nit.
The frequency of this output should be from 700Hz to 800Hz.

The following table is output characteristics of all outputs.

OUTPUT	CONDITION	VOLTAGE (V)	CURRENT (mA)	RIPPLE (mVp-p)
VGG		5.0±0.25	0.1 ~ 15	less than 100
VCC	IPON = High IPON = Low	5.0±0.25 less than 0.3	300 ~ 2800	less than 100
V+12	IPON = High IPON = Low	12.0±0.6 0±0.3	0 ~ 200	less than 150
V–12	IPON = High IPON = Low	–12.0±1.0 0±0.3	0 ~ –20	less than 150
V–5	IPON = High IPON = Low	–5.0±0.25 0±0.3	0 ~–20	less than 100
VCRT	PVCRT = High PVCRT = Low	5.0±0.25 less than 0.3	0 ~120	less than 100
VLCD	IPON = High IPON = Low	–20.7 ~–11.5 0±0.3	–10 ~–25	less than 200
VBKL	PVBKL = High PVBKL = Low	AC 35 ~ 100 0		

Table 6-3

NOTES 1) The control signals are from the CMOS IC powered by VGG, and the range of high is 4.0 to 5.25V, low is less than 0.5V.
2) PVCRT = High, PVBKL = High means IPON = High too.
3) The currents of the VCC is the peak current.
It is continuously supplied less than 1.6A.

(6) Input current of IPON, PVCRT, PVBKL

When IPON, PVCRT, PVBKL is high level (+4.0V) at on mode, the input current of them satisfy the Table 6-4.

	Input current
IPON	less than 1mA
PVCRT	less than 1mA
PVBKL	less than 1mA

Table 6-4

6-3. Battery recharge circuit

When the AC adapter or V_{EX} is supplied, if IPON is at low (the set is OFF), the charging characteristic of the battery is as shown in Fig. 6-2. To check the operation, provide a dummy resistor to the battery connector and check points A ~ D in Fig. 6-2 and Table 6-5.

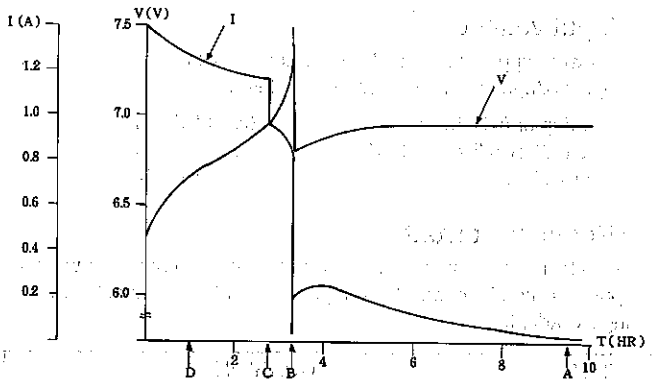


Fig. 6-2 Recharge characteristic

Table 6-5 Recharge circuit test point

Point	Voltage	Current	Remarks
A	6.85±0.05V	10mA	IPON at low, control with VR1.
B	7.5±0.2V	0.8~1.0A	Voltage/current are changed around this point.
C	6.85±0.1V	1~1.3A	Current reduces around this point.
D	6.5±0.2V	1.1~1.4A	Current is constant though voltage is varied.

Time required for charging the battery is about 8 hours when the set is OFF (IPON is at low), and 20 to 30 hours when the set is ON (IPON is at high).

CHAPTER 7. APPENDICES

7-1. μPD70208G Main CPU (V-40)

1. Features

1-1. High-performance 8-bit CPU

- 1M-byte memory space and 64K-byte I/O space
- Abundant memory addressing modes
- Fourteen 16-bit register sets
- Instruction set with 101 types of powerful instructions
- Bit field manipulation instructions
- Packed BDC arithmetic operation instructions
- Memory-memory high-speed block transfer instructions
- High-speed multiplication and division instructions by exclusive hardware
- High-speed effective address calculation by exclusive hardware
- A wealth of interrupt process functions
- μPD8080AF emulation mode
- Standby mode

1-2. Internal clock generator

1-3. Programmable wait function

1-4. Dynamic RAM refresh function

1-5. Timer/counter unit

- Three 16-bit counters
- Six programmable count modes
- binary/BCD count
- Multiple-latch commands

1-6. Serial control unit

- Asynchronous serial communication
- Clock rate: Baud rate x16, x64
- Baud rate: DC to 48.4k bits/sec.
- Character length: 7/8 bits
- Transfer stop bit: 1/2 bits

1-10. IEEE-796 bus compatible interface

1-11. CMOS

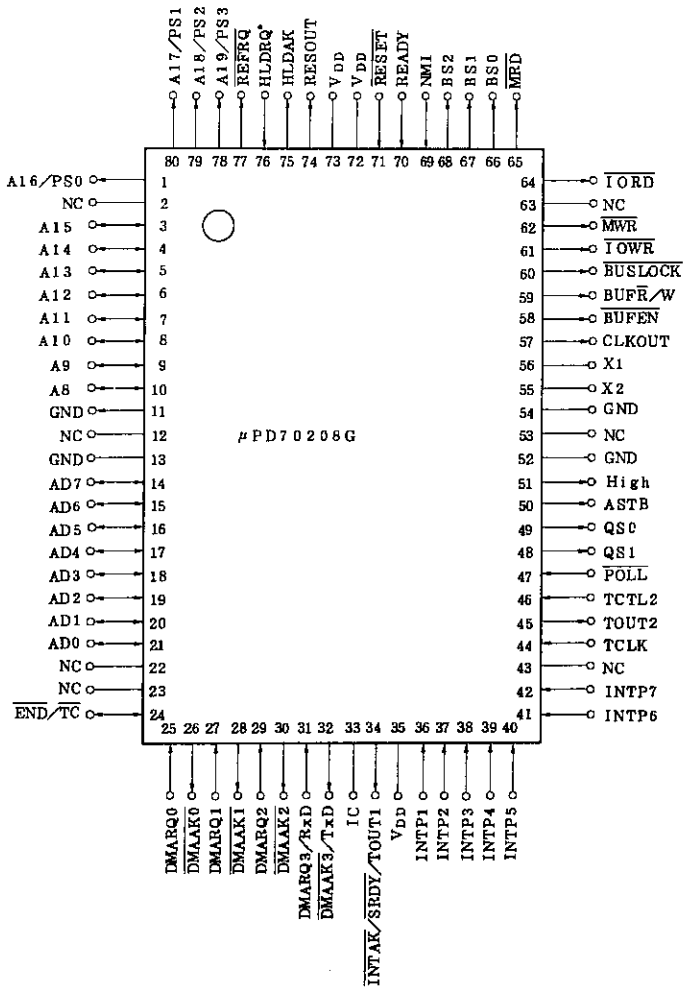
1-12. Low power consumption

1-13. Single power supply

1-14. 10-MHz clock

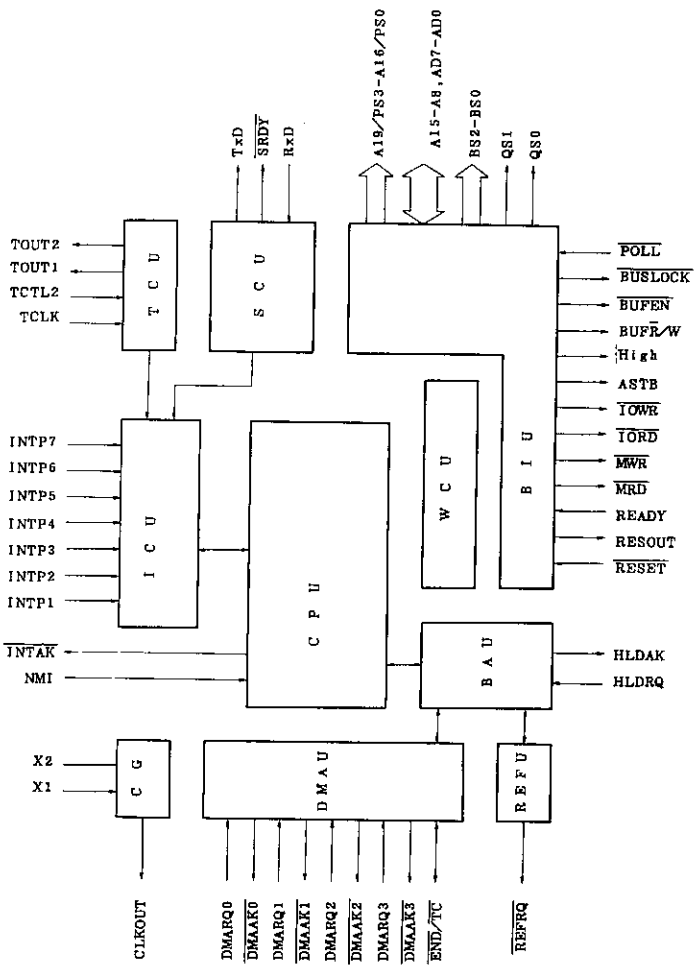
2. μPD70208G Pin Configurations

- 80-pin Plastic Flat Package (Top View)



NOTE: For μPD70208G, pins 3 to 10 are output only.

3. μPD70208G Block Diagram



4. Pin Function

4-1. AD7 to AD0 (address/data bus) ... 3-state input/output

These pins constitute a maltiplexed address/data bus that outputs the lower 8 bits of 20-bit address information and inputs/outputs 8-bit data on a time-division basis. These pins function as the address bus during T1 state of the bus cycle, and as the data bus during T2, T3, TW, and T4 states.
These pins become high impedance during hold acknowledge.

4-2. A15 to A8 (address bus) ... 3-state output

These pins output the middle 8 bits of 20-bit address information.
These pins become high impedance during hold acknowledge.

4-3. A19/PS3 to A16/PS0 (address bus/processor status) ... 3-state output

These are time-multiplexed output pins that output addresses and processor status signals.
These pins function as an address bus during T1 state of the bus cycle. They output processor status signals during T2, T3, TW, and T4 states.
When functioning as an address bus, these pins output the higher 4 bits of address information. All these pins output 0 during I/O access.
The processor status signal is output during both the memory and I/O accesses. The PS3 pin outputs 0 in native mode and when the cycle is neither DMA nor refresh; otherwise, it outputs 1. The PS2 pin outputs the content of the interrupt enable flag (IE).
The PS1 and PS0 pins indicate which segment is used by the current bus cycle.

Processor Status

A17/PS1	A16/PS0	Segment
0	0	Data segment 1 (DS1)
0	1	Stack segment (SS)
1	0	Program segment (PS)
1	1	Data segment 0 (DS0)

These pins become high impedance during hold acknowledge.

4-4. $\overline{\text{REFRQ}}$ (refresh request) ... Output

This is an output pin that outputs an active-low signal during T2, T3 and TW states of the refresh cycle.

4-5. HLDRQ (hold request) ... Input

This pin inputs a high-level signal when an external device requests that the address bus, address/data bus, and control bus be released. The priority of this signal is as follows: REFU (highest priority) > DMAU > HLDRQ > CPU > REFU (lowest priority).

4-6. HLDAK (hold acknowledge) ... Output

This signal indicates that the μPD70208/70216 has acknowledged the hold request signal (HLDRQ) and set the buses to the high-impedance state. When this signal is at the high level, therefore, the address bus, address/data bus, and control bus of 3-state output system become high-impedance state.
If a refresh request or DMA request with higher priority than the HLDAK signal occurs during hold acknowledge, HLDAK becomes inactive. Then the μPD70208G requests that the bus control be returned to it provided that the HLDRQ signal becomes inactive at the same time.

4-7. $\overline{\text{RESET}}$ (reset) ... Input

This is an active-low reset input pin and takes the precedence over all the other operations. The reset operation affects not only the CPU but also the on-chip peripherals. After the reset input is released, the CPU starts executing the program from address FFFF0H. The $\overline{\text{RESET}}$ input is also used to release the standby mode of the CPU.

4-8. RESOUT (reset output) ... Output

This pin synchronizes the asynchronous signal input to the $\overline{\text{RESET}}$ pin with the internal clock and then outputs it as an active-high signal. This signal can also be used as a system reset signal.

4-9. READY (ready) ... Input

The basic bus cycle of the μPD70208G requires four clocks. However, when the READY signal goes low (inactive) a wait state (TW) is inserted between T3 and T4 states and thus the bus cycle is extended. This function is used for memory or I/O whose access time is slow.
This signal is internally synchronized with the clock and supplied to each block. Then it is checked during T3 and TW states.
Other than by this signal, TW state can be also inserted by programmable wait function.

4-10. NMI (nonmaskable interrupt) ... Input

This pin inputs an interrupt request signal that cannot be masked by software.
This input signal is rising-edge triggered and is sampled in each clock cycle. When the current instruction has been executed, an interrupt assigned with No.2 vector is generated.
This interrupt is also used to release the standby mode of the CPU.

4-11. $\overline{\text{MRD}}$ (memory read) ... 3-state output

This signal becomes active (low level) when data is read from the memory. This signal also becomes active when the memory is refreshed by the on-chip refresh control unit or when data are transferred from the memory to I/O by the on-chip DMA control unit.
The $\overline{\text{MRD}}$ signal becomes active during T2, T3, and TW states of the bus cycle.
This pin becomes high impedance during hold acknowledge.

4-12. $\overline{\text{MWR}}$ (memory write) ... 3-state output

This signal becomes active (low level) when data are written to the memory. This signal also becomes active when data are transferred from the I/O to memory by the on-chip DMA control unit. When data are processed by the CPU, the $\overline{\text{MWR}}$ signal becomes active during T2, T3, and TW states. However, when data are processed by the DMA unit, the $\overline{\text{MWR}}$ signal becomes active during T3 and TW states.
This pin becomes high impedance during hold acknowledge.

4-13. $\overline{\text{IORD}}$ (I/O read) ... 3-state output

This signal becomes active (low level) when data are read from the I/O. However, if the I/O to be accessed is on the chip, it will not become active. The $\overline{\text{IORD}}$ signal also becomes active when data are transferred from the I/O to the memory by the on-chip DMA control unit. This signal becomes active during T2, T3 and TW states of the bus cycle.
This pin becomes high impedance during hold acknowledge.

4-14. $\overline{\text{IOWR}}$ (I/O write) ... 3-state output

This signal becomes active (low level) when data are written to the I/O. However, if the I/O to be accessed is on the chip, it will not become active. The $\overline{\text{IOWR}}$ signal also becomes active when data are transferred from the memory to I/O by the on-chip DMA control unit.
This signal becomes active during T2, T3, and TW states when data are processed by the CPU. However, when data are processed by the DMAU, the $\overline{\text{IOWR}}$ signal becomes active during T3 and TW states for normal write timing; T2, T3, and TW states for extended write timing.
This pin becomes high impedance during hold acknowledge.

4-15. ASTB (address strobe) ... Output

This signal is an active-high strobe signal that externally latches address information. This signal becomes active while the clock (CLKOUT) in T1 state of the bus cycle is at low level.
This pin outputs low-level signal during hold acknowledge.

4-16. $\overline{\text{BUSLOCK}}$ (bus lock) ... 3-state output

This signal is used to request the other master CPUs in the multiprocessor system not to use the system bus while the instruction following the BUSLOCK prefix is being executed or during interrupt acknowledge cycles.
During bus lock (i.e. $\overline{\text{BUSLOCK}}$ is active), hold request and DMA request are ignored, while refresh request is hold off.
This pin becomes high impedance during hold acknowledge.

4-17. $\overline{\text{POLL}}$ (poll) ... Input

The signal input to the $\overline{\text{POLL}}$ pin is checked by the POLL instruction. If the signal is at the low level, the program execution proceeds to the next instruction. If the $\overline{\text{POLL}}$ pin is at the high level, it is checked every five clocks until the $\overline{\text{POLL}}$ input goes low. These functions are used to synchronize the CPU program with the operations of external devices.

4-18. BUF$\overline{\text{R}}$/W (buffer read/write) ... 3-state output

This signal is output to determine the data transfer direction of an external bidirectional data buffer. If it is high level, data are output from the μPD70208G to the external device. If the signal is low level, data are input from the external device to the μPD70208G.
This pin becomes high impedance during hold acknowledge.

4-19. $\overline{\text{BUFEN}}$ (buffer enable) ... 3-state output

This signal is active low signal and is used as an output enable signal for the external bidirectional data buffer.
During T2 through T4 states of the read cycle and interrupt acknowledge cycle, it becomes active (low level). This signal also becomes active during T1 through T4 states of the write cycle.
However, the $\overline{\text{BUFEN}}$ pin will not become active when the internal I/O on the chip is accessed.
This pin becomes high impedance during hold acknowledge.

4-20. X2 and X1 (clock) ... Input

To use the internal clock generator, a crystal must be connected across the X2 and X1 pins. The oscillation frequency of the crystal to be connected should be 2 times the operating frequency.
If an external clock generator is to be used, the square wave of 2 times the operating frequency must be input to the X1 pin and the inverted signal of the X1 to the X2 pin.

4-21. CLKOUT (clock out) ... Output

This pin outputs the square wave clock that has one half the frequency of crystal frequency or X1 input frequency.

4-22. BS2 to BS0 (bus status) ... 3-state output

These pins output status signals that inform the external bus controller of the current bus cycle.
These signals become active during T1 and T2 states and are encoded as indicated in the table below. By decoding these encoded signals, the external bus controller can generate control signals by which to access the memory or I/O.
Only when CPU enters halt state, BS2 to BS0 indicates the CPU passive state one clock earlier than normal states.

BS2	BS1	BS0	Bus cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Program prefetch
1	0	1	Memory read*
1	1	0	Memory write (including DMA cycle)
1	1	1	CPU passive state

* In addition to the CPU read cycle, the "memory read cycle" includes the DMA cycle, DMA verify, and refresh cycle.

These pins become high impedance during hold acknowledge.

4-23. QS1 to QS0 (queue status) ... Output

These signals inform an external device (floating-point operation chip) of the CPU's internal instruction queue status.
The "queue status" means a status in which the execution unit (EXU) in the CPU accesses an instruction queue. The contents output to the QS1 and QS0 pins are valid only during one clock cycle immediately after the EXU has accessed the instruction queue.

QS1	QS0	Instruction queue status
0	0	No operation (no changing queue)
0	1	The first byte of an instruction is fetched.
1	0	The queue is empty.
1	1	The second or latter byte of the instruction is fetched.

The status signals are provided so that the floating-point operation chip can monitor the program execution status of the CPU and performs processing in synchronization with the CPU when the control is given to the chip by the FPO (floating point operation) instruction.

4-24. TOUT2 (timer output) ... Output

This is the output pin of the internal timer/counter unit (TCU). Of the three counters of the TCU, the result of the TCT#2 is output to this pin.

4-25. TCTL2 (timer control) ... Input

This is the control input pin of the internal timer/counter unit (TCU). Of the three counters, the TCT#2 is controlled by this input.

4-26. TCLK (timer clock) ... Input

This is the clock input pin of the internal timer/counter unit. However, the clock actually input to each counter is selected by software from either the clock input to this pin or the operating clock of the μPD70208G on which frequency division has been performed.

4-27. INTP7 to INTP1 (interrupt request from peripheral) ... Input

These seven pins input asynchronous interrupt requests to the internal interrupt control unit (ICU). Either edge-triggering (at the rising edge) or level-triggering (high level) of these input signals can be selected. These interrupt request inputs can be also used to release the standby mode of the CPU.
These pins have internal pull-up resistors.

4-28. $\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1 (interrupt acknowledge/serial ready/timer output) ... Output

This is a shared output pin for interrupt acknowledge signal, serial ready signal, and timer output (TCT#1). The interrupt acknowledge signal $\overline{\text{INTAK}}$ becomes active (low level) during T2, T3, and TW states of the interrupt acknowledge cycle of the CPU. The $\overline{\text{SRDY}}$ signal is output from the internal serial control unit (SCU) and becomes active (low level) when the receiver is enabled to receive data.
The TOUT1 signal is output from the internal timer/counter unit (TCU). Of the three counters, a result of the TCT#1 is output to this pin. The functions of this pin is selected by controlling the OPCN (on-chip peripheral connection) register in the μPD70208G by software.

4-29. $\overline{\text{DMAAK3}}$/TxD (DMA acknowledge/transmit data) ... Output

This is a shared pin and outputs the acknowledge signal for channel 3 of the DMA unit and serial data from the serial control unit (SCU).

The $\overline{\text{DMAAK3}}$ signal is active-low.

When this pin functions as the TxD pin, it becomes high level (marking) if there is no transmit data. When transmit data is set, the start bit (low level) is automatically output and then the set data is serially output. A parity bit and a stop bit (high level) are appended to the end of the each data. Whether to append the parity bit can be specified by program.

The μPD70208G's internal OPCN (on-chip peripheral connection) register controls the function of this pin (refer to 12.1. System I/O Area).

4-30. DMARQ3/RxD (DAM request/receive data) ... Input

This is a shared pin that inputs the request signal for channel 3 of the DMA unit and the serial data of the SCU.
The DMARQ3 signal is active-high.
When this pin functions as the RxD pin, a high-level (marking) signal is input to it when no data is transmitted. The RxD pin starts receiving data at the falling edge of the start bit.
The three pins described in Sections 4-28 through 4-30 can be specified in the following four ways by controlling register OPCN (on-chip peripheral connection) of the μPD70208G by software.

Pin election	DMAAK3/TxD	DMARQ3/RxD	INTAK/SRDY/TOUT1
1	$\overline{DMAAK3}$	DMARQ3	$\overline{INTAK}$
2	$\overline{DMAAK3}$	DMARQ3	TOUT1
3	TxD	RxD	$\overline{INTAK}$
4	TxD	RxD	$\overline{SRDY}$

4-31. $\overline{DMAAK2}$ to $\overline{DMAAK0}$ (DMA acknowledge) ... Output

These pins output the DMA acknowledge signals from channels 2 through 1 of the DMA unit.
These signals are active-low.

4-32. DMARQ2 to DMARQ0 (DMA request) ... Input

These pins input the DMA request signals to channels 2 through 0 of the DMA unit.
These signals are active-high.

4-33. $\overline{END}/\overline{TC}$ (end/terminal count) ... Input/output

This active-low pin controls termination of data transfer by DMA when the data transfer is performed by the DMA unit. When a low-level pulse ($\overline{END}$) is input to this pin during the DMA transfer, the DMA unit will terminate the ongoing DMA servicing. Also, when the number of DMA ransfers specified for each channel is complete, this pin outputs a low-level pulse ($\overline{TC}$).
Because this pin is an open-drain, a pull-up resistor must be externally connected.

4-34. V_{DD} (power supply)

This is a positive power supply pin.

4-35. GND (ground)

This is a ground pin (0V).

4-36. IC (internally connected)

Don't connect any signal with this pin and must be left open.

5. Functional Blocks

5-1. CPU (central processing unit)

The CPU consists of two independent processing units: BCU (bus control unit) and EXU (execution unit). Each of these two units performs the following function.

BCU ..... Prefetches instructions using instruction queues (the instruction queue is 4-byte for the μPD70208G.

EXU..... Processes data (executes microprograms).

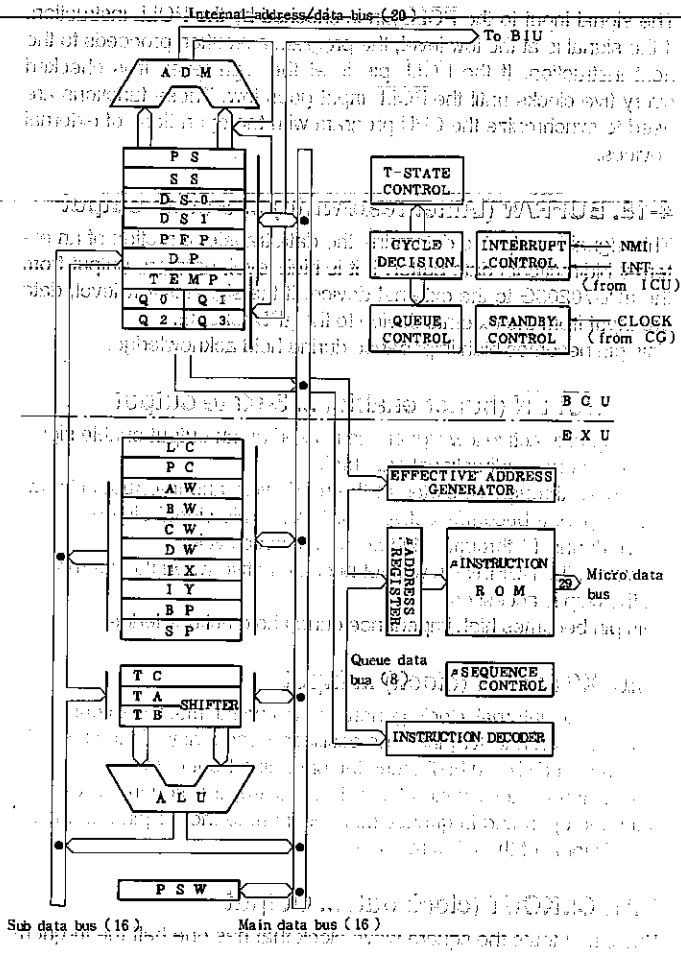


Fig. 5-1 μPD70208G CPU block diagram

5-2. BIU (bus interface unit)

The BIU controls the pins constituting the data bus, address bus, and control bus. These buses are used by three functional blocks: the CPU, DMAU (DMA control unit), and REFU (refresh control unit). The BIU synchronizes the $\overline{RESET}$ and READY inputs using the clock signal generated by the clock generator. The synchronized reset signal is active-high that is used in the μPD70208G as well as supplied to an external device via the $\overline{RESOUT}$ pin. The synchronized READY signal is supplied to the internal CPU, DMAU, and REFU.

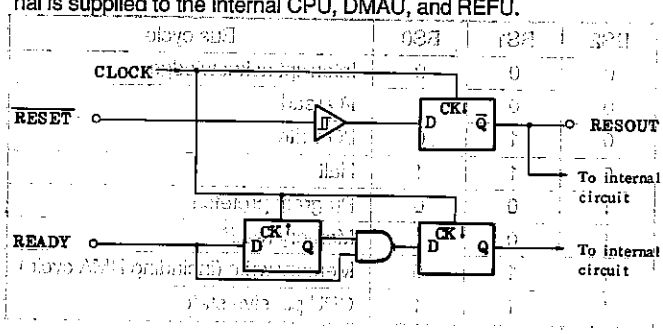


Fig. 5-2 Synchronization of $\overline{RESET}$ and READY

5-3. BAU (bus arbitration unit)

The BAU performs the bus control arbitration. The bus control priority is as follows:

REFU (highest priority) > DMAU > HLDRQ > CPU > REFU (lowest priority)

The REFU can take either the highest or lowest priority depending on the pending status of the refresh request. Even when a bus is used by a bus master, if another bus master with the higher priority requests the bus control, the BAU requests the current bus master to return the bus control by inactivating the acknowledge signal (i.e., bus acknowledge signal to the CPU, DMAU, or REFU, or the HLDAK signal to an external device). When the bus request signal (i.e., bus request signal from the CPU, DMAU, or REFU, or the HLDRQ signal from an external device) becomes inactive in response to this bus relinquish request, the BAU gives the bus control to the bus master with the higher priority.

When the bus control is sent between the internal bus masters, bus control request, acknowledge, relinquish request, and relinquish are efficiently performed.

5-4. CG (clock generator)

The CG generates clock signal one half the frequency of the crystal connected across the X1 and X2 pins and provides the clock to the CLKOUT pin and each functional block of the μ70208G. The duty cycle of the generated clock signal is 50%.

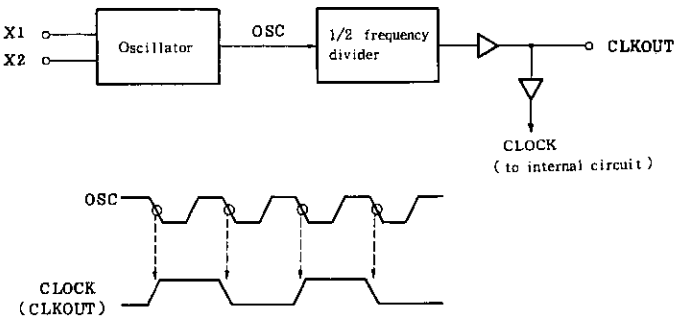


Fig. 5-3 Clock generator

5-5. REFU (refresh control unit)

The REFU generates refresh addresses and refresh request signals. By using these, the memory, if it is a dynamic RAM, can be refreshed.

5-6. WCU (programmable wait control unit)

The WCU has a function to insert up to three clocks of wait states TW to compensate for the process speeds of low-speed memories or I/O's. The number of clocks per wait state TW can be independently specified for CPU access, DMA access, and refresh access. Especially, when accessing the CPU, the memory space can be divided into three areas. These three areas and I/O can be independently specified.

5-7. TCU (timer/counter unit)

the TCU is a timer/counter unit. Three independent counters are provided in the TCU. The output signal of one of the counters is supplied to internal blocks whereas that of another one is supplied to external devices. The output of the last counter can be supplied to both internal and external devices.

5-8. SCU (serial control unit)

The SCU performs asynchronous serial communication.

5-9. ICU (interrupt control unit)

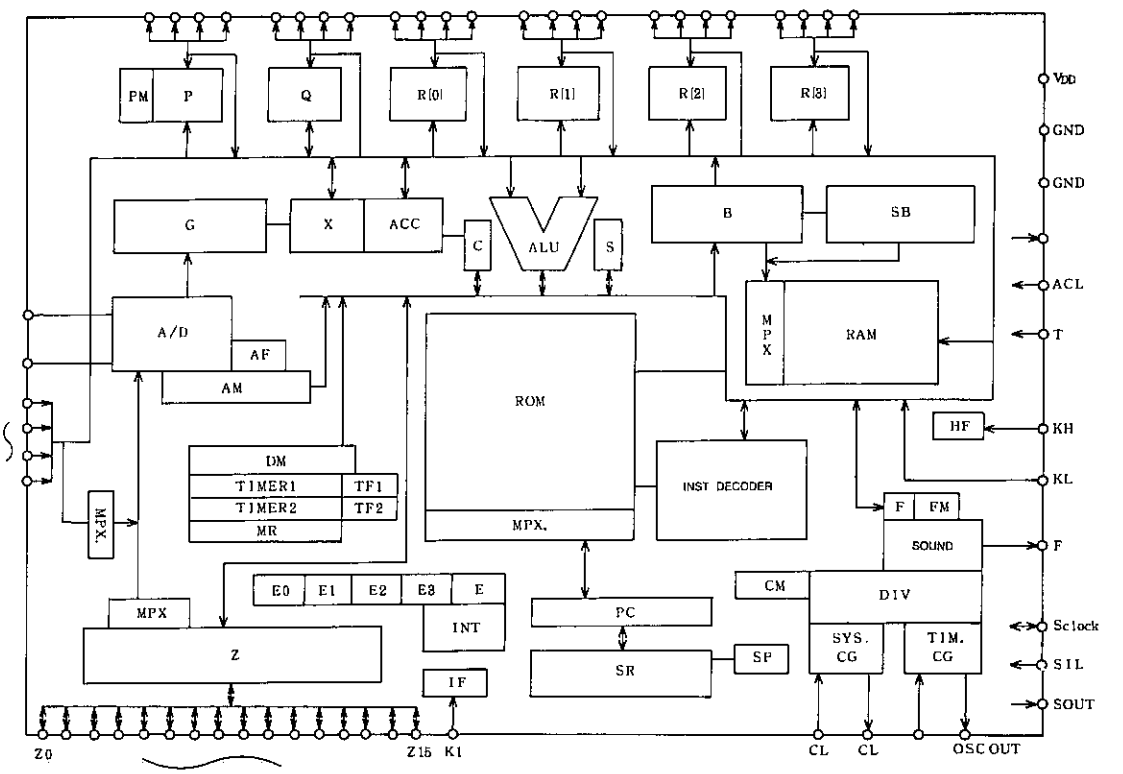
The ICU is an interrupt control unit, and arbitrates eight interrupt requests, generates an interrupt request that is to be sent to the CPU, and sends the interrupt vector number to the CPU. One of the eight interrupt request lines is not externally connected but it is connected to an output of the internal timer/counter.

5-10. DMAU (DMA control unit)

The DMAU is a DMA control unit and controls data transfer performed by using DMA (Direct Memory Access) between the memory and I/O.

7-2. LU57844P SUB CPU (SCM)

1) Block diagram



2) Sub CPU (SCM) pin description

Signal name	Pin	In/Out	Function
IPC0	P0	In/Out	Bi-directions: Host I/F port
IPC1	P1	In/Out	
IPC2	P2	In/Out	
IPC3	P3	In/Out	
PVCRT	Q00	Out	CRT Power switch
PVMDM	Q01	Out	Not used
PON (PVCC)	Q02	Out	VCC Power switch
KSTRA	Q03	Out	Key strobe line
KSEN0	R00	In	Key sense line (0 thru 7)
KSEN1	R01	In	
KSEN2	R02	In	
KSEN3	R03	In	
KSEN4	R10	In	
KSEN5	R11	In	
KSEN6	R12	In	
KSEN7	R13	In	
LED1	R20	Out	Caps Lock LED
LED2	R21	Out	Num Lock LED
LED3	R22	Out	Scrl Lock LED
*RESET	R23	Out	System Reset (active low)
FDN0 (SW7)	R30	Out	Not used
FDN1 (SW8)	R31	Out	Not used
COM1/2	R32	Out	COM1/*COM2 select
TKPDEW	R33	In	Ten-key-pad select switch (High)
KSTR0	Z0	Out	Key strobe line (0 thru 10)
KSTR1	Z1	Out	(KSTROBE0=SLP/RES key strobe)
KSTR2	Z2	Out	(KSTROBE1=ON SW strobe)
KSTR3	Z3	Out	
KSTR4	Z4	Out	
KSTR5	Z5	Out	
KSTR6	Z6	Out	
KSTR7	Z7	Out	
KSTR8	Z8	Out	
KSTR9	Z9	Out	(KSTROBE8, 9=Low Batt LED)
KSTR10	Z10	Out	(KSTROBE10=V-reference)
CPUHS	Z11	In	Host hand shake signal
SCMHS	Z12	Out	SCM hand shake signal
BKLIGHT	Z13	Out	Back-light control
KCLKOUT	Z14	Out	KEY I/F clock out
LB	Z15	Out	Low Battery Signal for HDD
KCLKIN	KI	In	KEY I/F clock in
ON/OFF	KH	In	ON SW sense
KDATAIN	KL	In	KEY I/F data in
LOWBAT0	KC0	An: Out/In	Low battery FATAL Level
LOWBAT1	KC1	An: Out/In	Low battery WARNING level
ACPOWER	KC2	An: Out/In	AC adaptor
*RI	KC3	In	Ring indicator
KDATAOUT	SOUT	Out	KEY I/F data out
SSPKR	F	Out	Low Battery Beep.
VCCHK	SIN	In	V_{CC} check

* means active low signal.

7-3. 8087
NUMERIC DATA COPROCESSOR
8087-1

- **High Performance Numeric Data Coprocessor**
- **Adds Arithmetic, Trigonometric, Exponential, and Logarithmic Instructions to the Standard 8086/8088 and 80186/80188 Instruction Set for All Data Types**
- **CPU/8087 Supports 7 Data Types: 16-, 32-, 64-Bit Integers, 32-, 64-, 80-Bit Floating Point, and 18-Digit BCD Operands**
- **Compatible with IEEE Floating Point Standard 754**
- **Adds 8 x 80-Bit Individually Addressable Register Stack to the 8086/8088 and 80186/80188 Architecture**
- **7 Built-In Exception Handling Functions**
- **MULTIBUS® System Compatible Interface**

The 8087 Numeric Data Coprocessor provides the instructions and data types needed for high performance numeric applications, providing up to 100 times the performance of a CPU alone. The 8087 is implemented in N-channel, depletion load, silicon gate technology (HMOS III), housed in a 40-pin package. sixty-eight numeric processing instructions are added to the 8086/8088, 80186/80188 instruction sets and eight 80-bit registers are added to the register set. The 8087 is compatible with the IEEE Floating Point Standard 754.

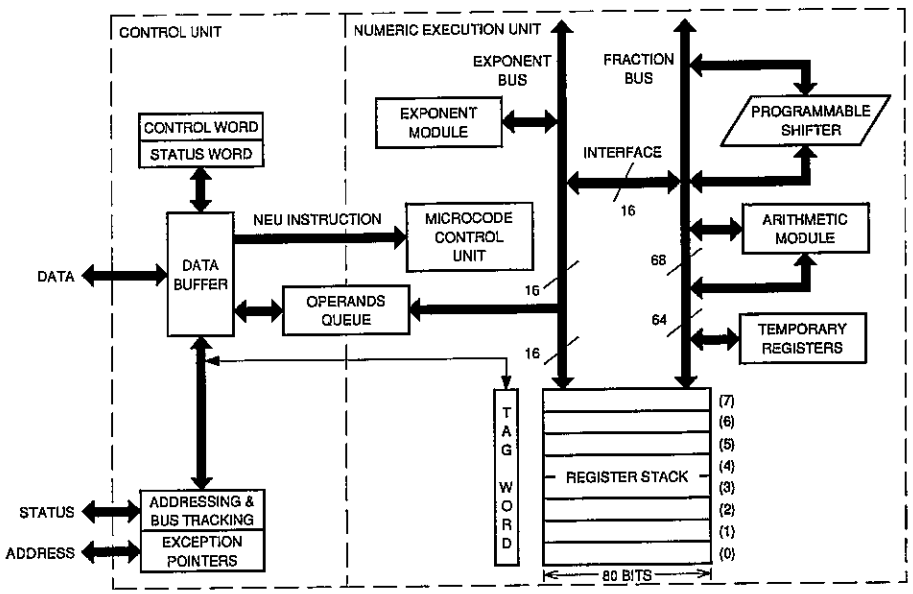


Figure 1. 8087 Block Diagram

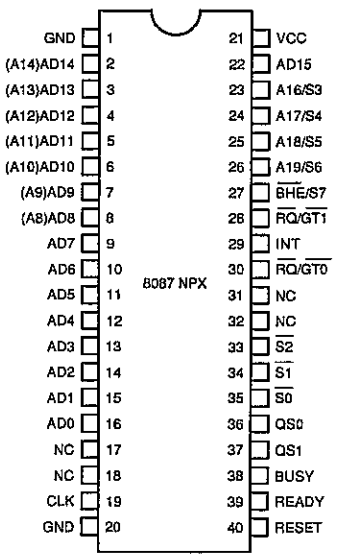


Figure 2. 8087 Pin Configuration

Table 1. 8087 Pin Description

Symbol	Type	Name and Function
AD15 – AD0	I/O	**ADDRESS DATA:** These lines constitute the time multiplexed memory address (T_1) and data (T_2, T_3, T_W, T_4) bus. A0 is analogous to the $\overline{BHE}$ for the lower byte of the data bus, pins D7 – D0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory operations. Eight-bit oriented devices tied to the lower half of the bus would normally use A0 to condition chip select functions. These lines are active HIGH. they are input/output lines for 8087-driven bus cycles and are inputs which the 8087 monitors when the CPU is in control of the bus. A15 – A8 do not require an address latch in an 8088/8087 or 80188/8087. the 8087 will supply an address for the T_1 – T_4 period.
A19/S6, A18/S5, A17/S4, A16/S3	I/O	**ADDRESS MEMORY:** During T_1 these are the four most significant address lines for memory operations. During memory operations, status information is available on these lines during T_2, T_3, T_W, and T_4. For 8087-controlled bus cycles, S6, S4, and S3 are reserved and currently one (HIGH), while S5 is always LOW. These lines are inputs which the 8087 monitors when the CPU is in control of the bus.
BHE/S7	I/O	**BUS HIGH ENABLE:** During T_1 the bus high enable signed ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15 – D8. Eight-bit-oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read and write cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T_2, T_3, T_W, and T_4. The signal is active LOW. S7 is an input which the 8087 monitors during the CPU-controlled bus cycles.
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	I/O	**STATUS:** For 8087-driven, these status lines are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ 0 (LOW) X X Unused 1 (HIGH) 0 0 Unused 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive Status is driven active during T_4, remains valid during T_1 and T_2, and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller (or the 82188 Integrated Bus Controller with an 80186/80188 CPU) to generate all memory access control signals. Any change in $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These signals are monitored by the 8087 when the CPU is in control of the bus.
$\overline{RQ}/\overline{GT0}$	I/O	**REQUEST/GRANT:** This request/grant pin is used by the 8087 to gain control of the local bus from the CPU for operand transfers or on behalf of another bus master. It must be connected to one of the two processor request/grant pins. The request/grant sequence on this pin is as follows: 1. A pulse one clock wide is passed to the CPU to indicate a local bus request by either the 8087 or the master connected to the 8087 $\overline{RQ}/\overline{GT1}$ pin. 2. The 8087 waits for the grant pulse and when it is received will either initiate bus transfer activity in the clock cycle following the grant or pass the grant out on the $\overline{RQ}/\overline{GT1}$ pin in this clock if the initial request was for another bus master. 3. The 8087 will generate a release pulse to the CPU one clock cycle after the completion of the last 8087 bus cycle or on receipt of the release pulse from the bus master on $\overline{RQ}/\overline{GT1}$. For 80186/80188 systems the same sequence applies except $\overline{RQ}/\overline{GT}$ signals are converted to appropriate HOLD, HLDA signals by the 82188 Integrated Bus Controller. This is to conform with 80186/80188's HOLD, HLDA bus exchange protocol. Refer to the 82188 data sheet for further information.

Table 1. 8087 Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{RQ}/\overline{GT}1$	I/O	**REQUEST/GRANT:** This request/grant pin is used by another local bus master to force the 8087 to request the local bus. If the 8087 is not in control of the bus when the request is made the request/grant sequence is passed through the 8087 on the $\overline{RQ}/\overline{GT}0$ pin one cycle later. Subsequent grant and release pulses are also passed through the 8087 with a two and one clock delay, respectively, for resynchronization. $\overline{RQ}/\overline{GT}1$ has an internal pullup resistor, and so may be left unconnected. If the 8087 has control of the bus the request/grant sequence is as follows: 1. A pulse 1 CLK wide from another local bus master indicates a local bus request to the 8087 (pulse 1). 2. During the 8087's next T_4 or T_1 a pulse 1 CLK wide from the 8087 to the requesting master (pulse 2) indicates that the 8087 has allowed the local bus to float and that it will enter the "RQ/GT acknowledge" state at the next CLK. The 8087's control unit is disconnected logically from the local bus during "RQ/GT acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 8087 (pulse 3) that the "RQ/GT" request is about to end and that the 8087 can reclaim the local bus at the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW. For 80186/80188 system, the $\overline{RQ}/\overline{GT}1$ line may be connected to the 82188 Integrated Bus Controller. In this case, a third processor with a HOLD, HLDA bus exchange system may acquire the bus from the 8087. For this configuration, $\overline{RQ}/\overline{GT}1$ will only be used if the 8087 is the bus master. Refer to 82188 data sheet for further information.
QS1, QS0	I	**QS1, QS0:** QS1 and QS0 provide the 8087 with status to allow tracking of the CPU instruction queue. **QS1** **QS0** 0 (LOW) 0 No Operation 0 1 First Byte of Op Code from Queue 1 (HIGH) 0 Empty the Queue 1 1 Subsequent byte from Queue
INT	O	**INTERRUPT:** This line is used to indicate that an unmasked exception has occurred during numeric instruction execution when 8087 interrupts are enabled. This signal is typically routed to an 8259A for 8086/8088 systems and to INT0 for 80186/80188 systems. INT is active HIGH.
BUSY	O	**BUSY:** This signal indicates that the 8087 NEU is executing a numeric instruction. It is connected to the CPU"s $\overline{TEST}$ pin to provide synchronization. In the case of an unmasked exception BUSY remains active until the exception is cleared. BUSY is active HIGH.
READY	I	**READY:** READY is the acknowledgement from the addressed memory device that it will complete the data transfer. The RDY signal from memory is synchronized by the 8284A Clock Generator to form READY for 8086 systems. For 80186/80188 systems, RDY is synchronized by the 82188 Integrated Bus Controller to form READY. This signal is active HIGH.
RESET	I	**RESET:** RESET causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. RESET is internally synchronized.
CLK	I	**CLOCK:** The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}		**POWER:** V_{CC} is the +5V power supply pin.
GND		**GROUND:** GND are the ground pins.

NOTE: For the pin descriptions of the 8086, 8088, 80186 and 80188 CPUs, reference the respective data sheets (8086, 8088, 80186, 80188).

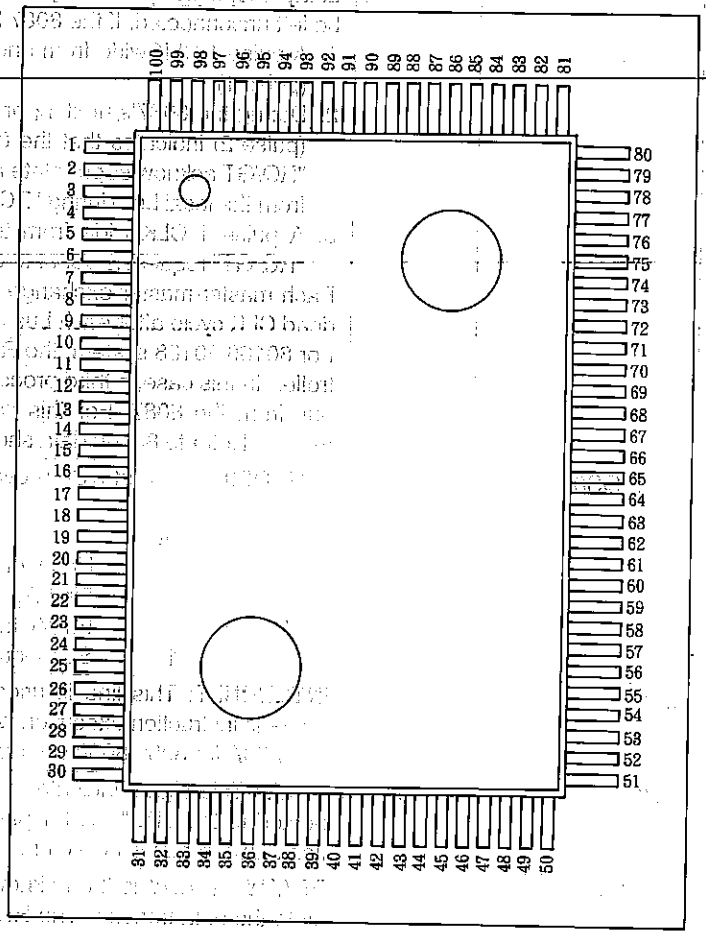
7-4. TC8566F Floppy Disk Controller II

1) General

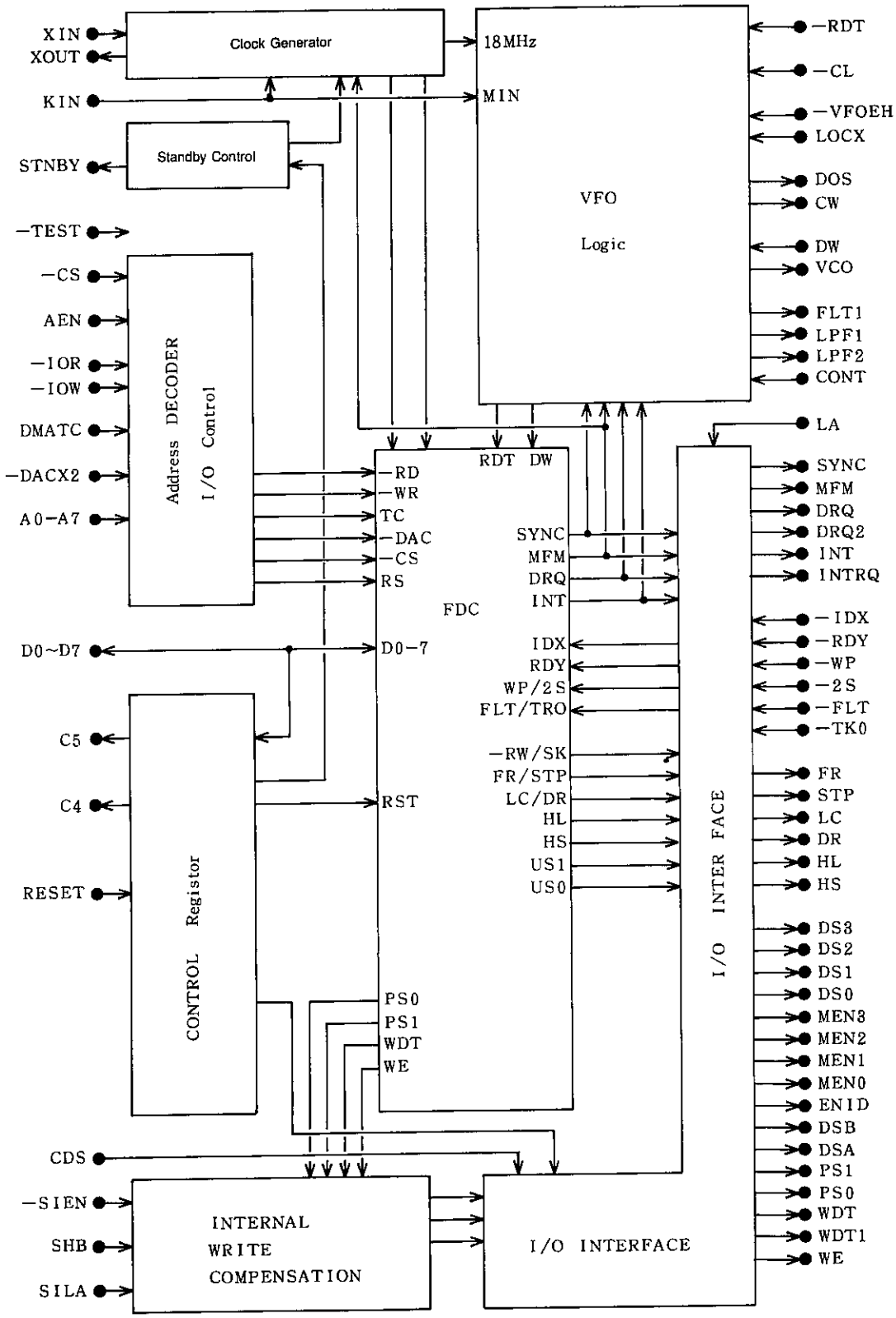
The TC8586F is a floppy disk control microchip designed to interface four floppy disk unit with the CPU. In this chip is implemented a high performance VFO circuitry and peripheral logic circuitry.

2) Features

- ❑ Silicon gate CMOS
- ❑ Single 5V supply
- ❑ 100-pin flat package
- ❑ Internal oscillator
- ❑ Internal VFO
- ❑ Internal standby circuit
- ❑ FD/MFD selection
- ❑ FM/MFM recording mode
- ❑ Internal write compensation
- ❑ Motor enable output control
- ❑ Internal I/O address decoder
- ❑ Multi-sector, multi-track
- ❑ Simultaneous seek, 4 drives
- ❑ Drive interface Schmitt trigger input
- ❑ Programmable step rate
- ❑ IBM compatible track format
- ❑ Internal CRC generation and check (X16+X12+X5+1)
- ❑ Programmable head load and unload time
- ❑ Data scan function
- ❑ DMA/non-DMA data transfer



3) TC8566F block diagram



4) Signal description

Pin No.	Signal name	In/Out	Description
1	C6	Out	Control register C6 output
2	$\overline{IOR}$	In	Signal used to transfer data onto the data bus from the FDC.
4	$\overline{IOW}$	In	Control signal to transfer data from the data bus to FDC.
5	A0	In	Address signal
6	A1	In	
7	A2	In	
8	A3	In	
9	A4	In	
10	A5	In	
11	A6	In	
12	A7	In	
13	$\overline{CS}$	In	FDC chip select
14	AEN	In	Address enable from the CPU
15	D0	In/Out	Bidirectional 8-bit data bus
16	D1	In/Out	
17	D2	In/Out	
18	D3	In/Out	
19	D4	In/Out	
20	D5	In/Out	
21	D6	In/Out	
22	D7	In/Out	
23	DRQ2	Out	DMA request. Output to delay DRQ. The signal is at a low level when the control register ENID bit is 0.
24	INTRQ	Out	Interrupt request issued by the FDC. The signal is at a low level when the control register ENID bit is 0. This signal stays low.
25	INT	Out	Interrupt request issued from the FDC.
26	DRQ	Out	DMA request
27	[VSS]	G	FDC digital ground
28	AG	G	VCO analog ground
32	$\overline{DACK2}$	In	DMA cycle becomes valid with a low state of this as input at DMA transfer.
33	DMATC	In	Indicates end of DMA during DMA transfer.
34	CONT	In	VCO control voltage input
35	$\overline{TEST}$	In	Test input with a pullup resistance. Normally, not to be connected or fixed high.
36	VCO	In/Out	Test input in the test mode, but normally output. To be connected with the low gain side filter.
37	LPF2	Out	Output connected to LPF of the PLL circuit. Selected after leading frequency. To be connected with the low gain side filter.
38	LPF1	Out	Output connected to LPF of the PLL circuit. Selected after leading frequency. To be connected with the high gain side filter.
39	CW	Out	Test input. Not to be connected.
40	$\overline{DW}$	In	Data window input signal required when using external VFO circuit. Normally, low or high fixed.
41	FLT1	Out	Test input used to indicate filter switching. Not to be connected.
42	DOS	Out	Test input. Not to be connected.
43	LOCK	In	Test input with a pullup resistance. Normally, not to be connected or fixed high.
44	$\overline{RDT}$ (RDT)	In	Data read signal from the floppy disk drive. When the external VFO circuit is used, it is a data read signal (RDT) input from the external VFO circuit.
45	XOUT	Out	Crystal oscillator inverter amp output pin.
46	XIN	In	Crystal oscillator inverter amp input pin which is used for the 16MHz external clock.
47	$\overline{VFOEN}$	In	Internal VFO select signal. Internal VFO is selected with a low state of signal and the external VFO is chosen with a high state of signal.
48	MIN	In	Used to select the standard floppy disk and mini-floppy disk. Low: Standard floppy disk High: Mini-floppy disk
49	MFM	Out	High: MFM mode Low: FM mode
53	$\overline{CL}$	In	This pin incorporates a pullup resistance and is used to reset the internal clock generator and VFO flip-flop with a low state of signal. Normally, not to be connected or fixed high.
54	[VSS]	G	FDC digital ground
55	SYNC	Out	Indicates that the FDC is in reading action.

Pin No.	Signal name	In/Out	Description
56	WDT1	Out	FDD write data compensation output signal. Active low when LA is high.
57	WE	Out	Used to direct the FDD to write data. Active low when LA is high.
58	HS	Out	Head 0 is selected with a low state of this signal when LA is at a low level. Head 1 is selected with a low state of this signal when LA is at a low level.
59	HL	Out	Used to direct the FDD to load the read/write head on the disk. Active low when LA is at a low level.
60	MEN3	Out	Number 3 unit drive motor enable, active low when LA is at a high level.
61	MEN2	Out	Number 2 unit drive motor enable, active low when LA is at a high level.
62	MEN1	Out	Number 1 unit drive motor enable, active low when LA is at a high level.
63	MEN0	Out	Number 0 unit drive motor enable, active low when LA is at a high level.
64	[VSS]	G	FDC digital ground
65	[VDD]	V	Single 5V supply. All VDD lines connected to +5V.
66	DS3	Out	Indicates that the number 3 unit is selected, active low when LA is at a high level.
67	DS2	Out	Indicates that the number 2 unit is selected, active low when LA is at a high level.
68	DS1	Out	Indicates that the number 1 unit is selected, active low when LA is at a high level.
69	DS0	Out	Indicates that the number 0 unit is selected, active low when LA is at a high level.
70	STP	Out	Used to deliver step pulse to move the head to another cylinder, active low when LA is at a high level.
71	FR	Out	Used to reset a fault of the FDD, active low when LA is at a high level.
72	LC	Out	Indicates that the read/write head is on the cylinder position after the 43rd cylinder, active low when LA is at a high level.
73	DR	Out	Indicates the direction of the head in the seek mode. Seeks towards disk periphery with a low state of this signal and disk center with a high state of this signal when LA is at a low level. Seeks towards the disk periphery with a high state of this signal and disk center with a low state of this signal when LA is at a high level.
74	[VSS]	G	FDC digital ground
75	[VDD]	V	Single +5V supply. All VDD lines are connected to +5V.
76	$\overline{IDX}$	In	Indicates the start point of track on the disk.
77	$\overline{RDY}$	In	Indicates that the FDD is ready.
80	$\overline{WP}$	In	Indicates that the disk is write protected.
81	$\overline{2S}$	In	Indicates the use of two-sided floppy disk.
82	$\overline{FLT}$	In	Indicates that the FDD is at a fault.
83	$\overline{TK0}$	In	Indicates that the head is on track 0.
84	PS1	Out	Indicates write compensation information in the MFM mode.
85	PS0	Out	Late if PS0 is at a low and PS1 at a high. Early if PS0 is at a high and PS1 at a low. Normal if PS0 is at a low and PS1 at a low.
86	DSB	Out	FDD select signal. #0 drive: DSB=low, DSA=low #1 drive: DSB=low, DSA=high #2 drive: DSB=high, DSA=low #3 drive: DSB=high, DSA=high
87	DSA	Out	
88	LA	In	Determines logic of the drive side output. WDT1, WE, HG, HL, MEN0 ~ MEN3, DS0 ~ D53, STP, FR, LC, DR are active low with a high state of this signal.
90	[VDD]	V	Single +5V supply. All VDD lines are connected to +5V.
92	CDS	In	Control register DSB and DSA are selected as drive select signal with a high state of this signal. Internal FDC block US1 and US0 are selected as drive select signal with a low state of this signal.
93	RESET	In	Resets the contents of control register.
94	SHB	In	Used to indicate rate of shift for the write.
95	SHA	In	Compensation circuit. 125ns when SHB is low and SHA low. 250ns when SHB is low and SHA high. 375ns when SHB is high and SHA low. 500ns when SHB is high and SHA high. One half of the above values is used for the standard floppy disk.
96	$\overline{SHEN}$	In	Used to set SHB and SHA valid. Rate of shift becomes 0 for the write compensation circuit when the signal is at a high level.
97	STNBY	Out	Indicates that the FDC is at standby. WDT1, WE, HG, HL, MEN0 ~ MEN3, DS0 ~ DS3, STP, FR, LC, DR are active low when in the standby mode.
98	WDT	Out	FDD write data composed of clock bits and data bits.
99	ENID	Out	Control register ENID bit output.
100	C4	Out	Control register C4 output.

7-5. INS82C50A asynchronous communication element

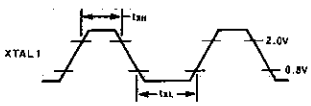
1. General description and features

- Enhances interface with almost any microprocessor
- Add/delete of suffixed bit(s) (START, STOP, PARITY) for async communication
- Full double buffer method that does not require precise synchronization
- Independently controlled transmit, receive, line status, data set interrupts
- 1 – (216 – 1) divided programmable buad rate generator (internal 16 x clock generation)
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, DCD)
- Serial interface format full compatible
  - 5, 6, 7, 8 bits character size
  - Even, off, non parity
  - 1, 1-2/1, stop bits
  - Baud rate generation (DC – 56K bauds)
- Illogical start bit detection
- Variety of status information
- Bidirectional data bus, control bus directly controlled tri-state TTL driver
- Start and detect of line break
- Internal self-diagnostics
  - Device internal loopback control
  - Break, parity, overrun, framing error simulation
- Interrupt controlled with priority

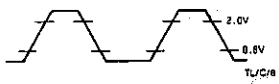
Timing waveforms

All waveforms are explained in reference to bit 0 and 1.

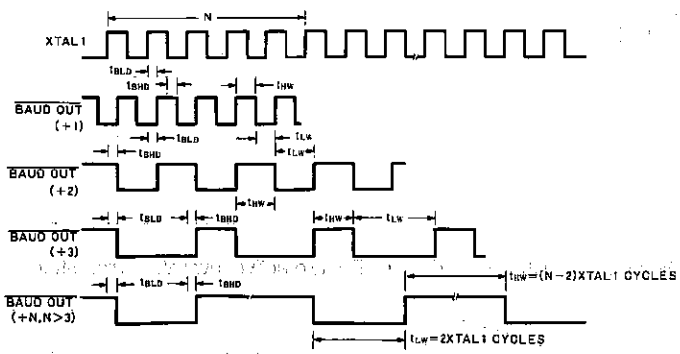
Internal clock (3.1MHz, max.)



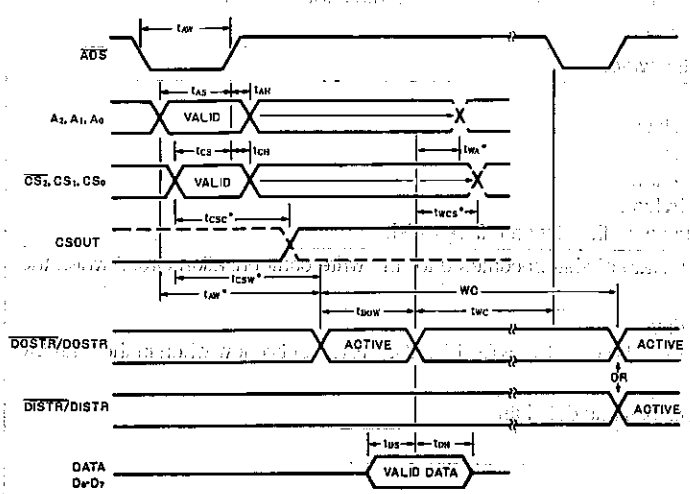
AC test point



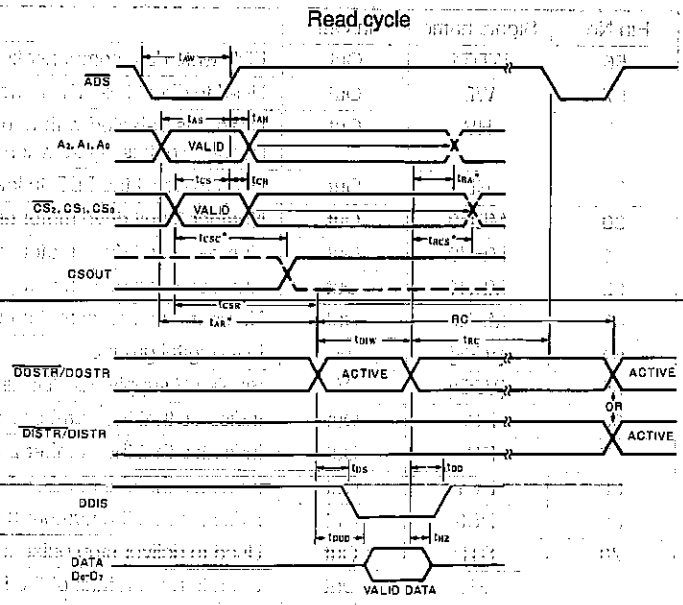
BAUDOUT timing



Write cycle

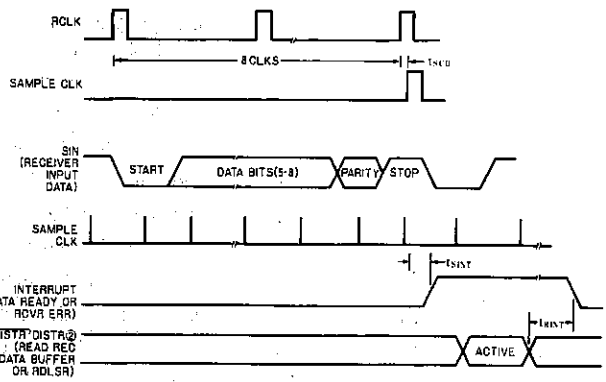


Read cycle

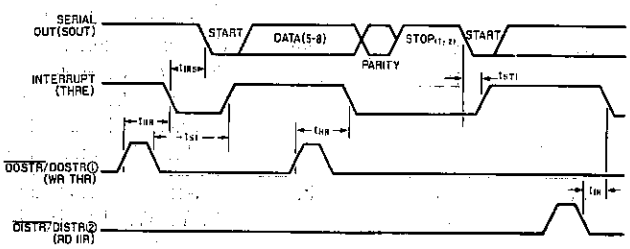


ADS fixed to low level for measurement

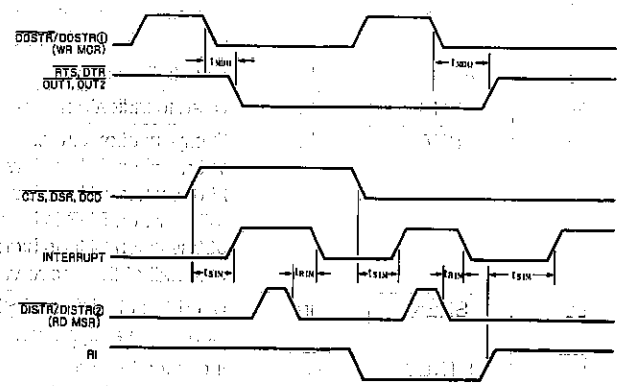
Receiver timing



Transmitter timing

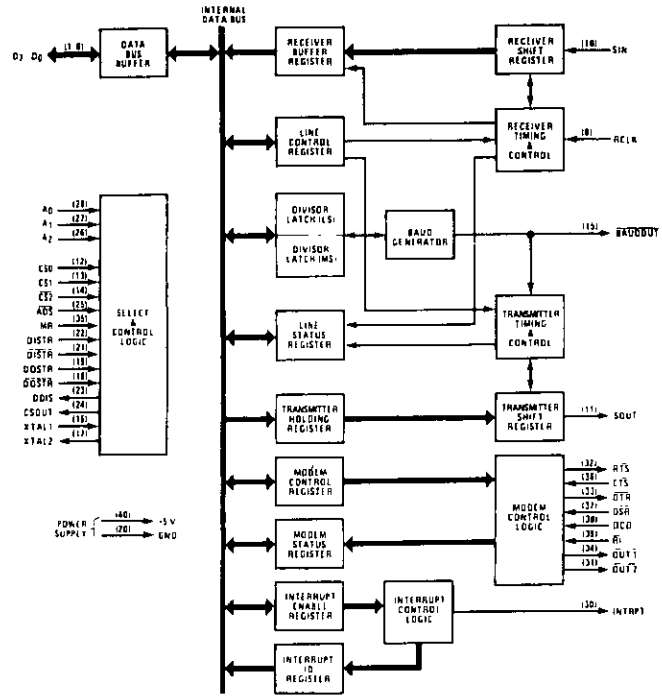


Modem control timing



① : Refer to write cycle.
② : Refer to read cycle.

2. Block diagram



3. Pin description

Discussed below are functions of I/O signal lines. Some of those relate to the internal circuitry.

NOTE: In the discussion, low level signal means logic 0 and high level signal logic 1.

INPUT SIGNALS

Chip select (CS0, CS1, $\overline{CS2}$, pin-12 to pin-14)

The chip is selected with a high state of CS0 and CS1 and low state of $\overline{SC2}$. Chip is selected by latching the decoded chip select signal at a trail edge of the address strobe signal $\overline{ADS}$. When the chip is selected, communication is enabled between the ACE and the CPU.

Data input strobe (DISTR, $\overline{DISTR}$, pin-22 and 21)

When DISTR input is at a high or $\overline{DISTR}$ is at a low after the chip was selected, status information from the ACE selected register and data are read by the CPU.

NOTE: When either $\overline{DISTR}$ or DISTR is set active, the data will be read from the ACE to the CPU. Therefore, $\overline{DISTR}$ must be set low or DISTR low when the line is not used.

Data output strobe (DOSTR, $\overline{DOSTR}$, pin-19 and 18)

When DOSTR is at a high or $\overline{DOSTR}$ is at a low after the chip was selected, data or control word are written to thee ACE selected register.

NOTE: Either $\overline{DOSTR}$ or DOSTR must be set active to write to ACE. Therefore, DOSTR must be set low or $\overline{DOSTR}$ high when the line is not used.

Address strobe ($\overline{ADS}$, pin-25)

When this line is low, the register select signals (A0, A1, A2) and chip select signals (CS0, CS1, $\overline{CS2}$) are latched.

NOTE: The ADS input is used when register select signals (A0, A1, A2) and chip select signals (CS0, CS1, $\overline{CS2}$) are not stable. The signal must be set low for such this that this input is not required.

DLAB	A2	A1	A0		Register
0	0	0	0	R	Receive buffer (holding register)
0	0	0	0	W	Trensmit buffer (holding register)
0	0	0	1		Interrupt mask
X	0	1	0		Interrupt ID
X	0	1	1		Line control
X	1	0	0		Modem control
X	1	0	1	R	Line status
X	1	1	0	R	Modem status
X	1	1	1		Scratch pad
1	0	0	0		Baud rate divide register, LSB
1	0	0	1		Baud rate divide register, MSB

R: Read only register
W: Write only register

Register select (A0, A1, A1, pin-26 to pin-28)

Used to select the register during read or write.

As shown in the table, the divisor latch access bit (DLAB) which is the most significant bit of the line control register relates to register selection. In order to access the baud rate generator divisor latch, the DLAB bit must be set 1 by the system software.

Master reset (MR, pin-35)

A TTL compatible schmitt trigger buffer that has a 0.5 (standard) hysteresis is implemented in this input line. When the line is at a high level, all registers and control logics are cleared, except for the receiver buffer, transmit holding, and divisor latch. Also, the output signals (SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) change as in Table-1.

Receiver clock (RCLK, pin-9)

A 16 x clock input line that has a receiver circuit.

Serial input (SIN, pin-10)

Serial data input line from the communication link (peripheral device, modem, data terminal).

Clear to send ($\overline{CTS}$, pin-36)

CTS is a modem control signal whose state is tested by referring to the bit 4 (CTS) of the modem status register. The bit 0 (DCTS) of the modem status register is set 1 when there was a change in the state of the $\overline{CTS}$ input in the period that this register is read after the modem status register was read. The $\overline{CTS}$ input does not affect the transmitter at all.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the CTS bit of the modem status register.

Data set ready ($\overline{DSR}$, pin-37)

A low on this line indicates that the modem or the data set is ready to receive and send. For $\overline{DSR}$ is a modem control input, its state can be tested by referring to the bit 5 (DSR) of the modem status register. The bit 1 (DDSR) of the modem status register is set 1 when there was a change in the state of the $\overline{DSR}$ input in the period that this register is read after the modem status register was read.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the DSR bit of the modem status register.

Data carrier detect ($\overline{DCD}$, pin-38)

A low on this line indicates that data carrier is detected by the modem or data set. For $\overline{CD}$ is a modem control input, its state can be tested by referring to the bit 7 (DCD) of the modem status register. The bit 3 (DDCD) of the modem status register is set 1 when there was a change in the state of the $\overline{DCD}$ input in the period that this register is read after the modem status register was read.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the $\overline{DCD}$ bit of the modem status register.

Ring indicator 8-$\overline{RI}$, pin-39)

A low on this line indicates that ring is detected by the modem or data set. For $\overline{RI}$ is a modem control input, its state can be tested by referring to the bit 6 (RI) of the modem status register. The bit 2 (TERI) of the modem status register is set 1 when there was a change in the state of the $\overline{RI}$ input in the period that this register is read after the modem status register was read.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the $\overline{RI}$ bit of the modem status register.

VCC: pin-40
+5V supply
VSS: pin-20
GND (0V), reference voltage ground

OUTPUT SIGNAL DESCRIPTION

Data terminal ready ($\overline{DTR}$, pin-33)

A low on this line indicates that the ACE is enabled to communicate with the modem or the data set. $\overline{DTR}$ turns active when the bit 0 (DTR) of the modem control register is set by the program. This output is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Request to send ($\overline{RTS}$, pin-32)

A low on this line indicates that the ACE is enabled to send data to the modem or the data set. $\overline{RTS}$ turns active when the bit 1 (RTS) of the modem control register is set by the program. This output is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Output-1 ($\overline{OUT1}$, pin-34)

A general purpose output line which goes active low when the bit 2 (OUT1) of the modem control register is set by the program. $\overline{OUT1}$ is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Output-2 ($\overline{OUT2}$, pin-31)

A general purpose output line which goes active low when the bit 3 (OUT2) of the modem control register is set by the program. $\overline{OUT2}$ is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Chip select out (CSOUT, pin-24)

A high level signal is issued on this line when CS0, $\overline{CS1}$, and $\overline{SC2}$ are set high to select chip. Data are not sent out until CSOUT goes high.

Driver select out (DDIS, pin-23)

Goes low when ACE data are read by the CPU. When the CPU is reading other than data, the line is kept high. Used to disable an external data transceiver which is established on the data bus D7 ~ D0 between the CPU and the ACE.

Baud out ($\overline{BAUDOUT}$, pin-15)

The 16 x clock used in the ACE transmitter circuitry is sent out. The clock frequency is the value the basic clock input is divided by the value set in the baud rate divisor latch. When the $\overline{BAUDOUT}$ output is connected to the RCLK input, it can also be used for the receiver clock.

Interrupt (INTRPT, pin-30)

Goes active when one of receiver error flag, receive data available, transmitter holding register empty, and modem status interrupts is requested. If the corresponding IER bit was set, the line goes high. The INTR output is reset low after the master reset is conducted or an adequate interrupt service is done.

Serial output (SOUT, pin-11)

Through this line is sent out the serial data to the communication link (modem or data set). The line is set high (MARK) when the master reset is conducted.

INPUT/OUTPUT PIN DESCRIPTION

Data bus (D7 ~ D0, Pin-1 to -8)

An eight line tri-state input/output used to carry bidirectional data communication between the ACE and the CPU. Data, control word, and status information are transferred via this data bus.

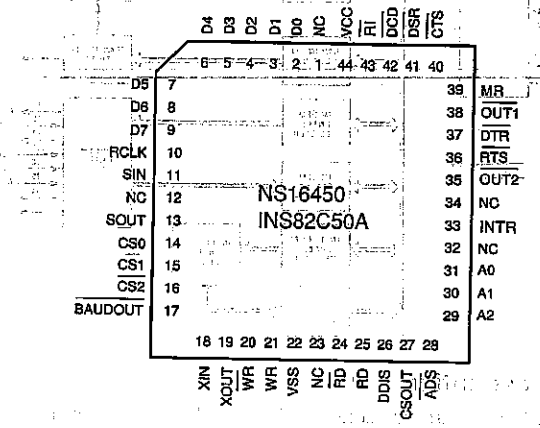
External clock input/output (XTAL1, XTAL2, pin-16 and 17)

Connected to the basic clock input (crystal oscillator or external clock).

NOTE: Pin numbers described are for the dual in-line package.

Pin Configuration

PLCC Package



Top view

7-6. LZ95H12 (Gate array)

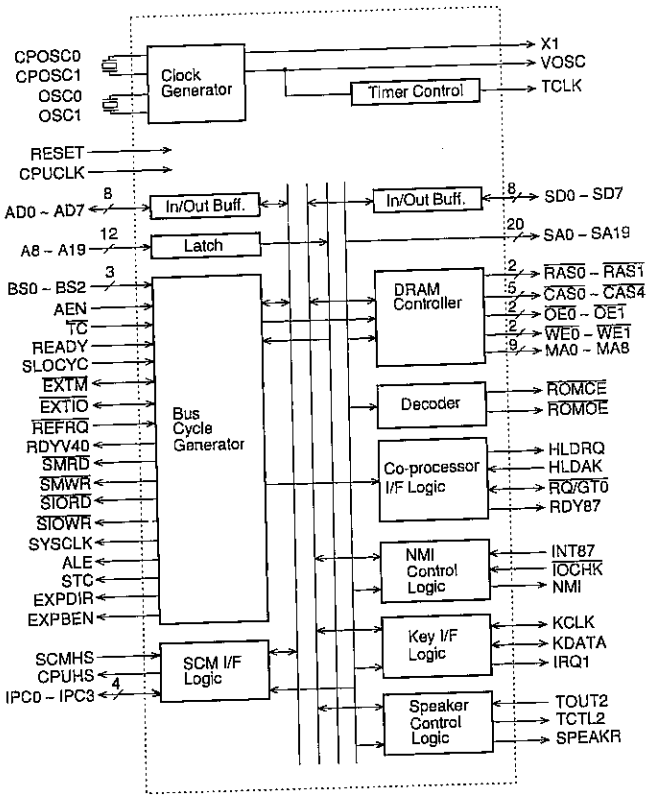
General

The LZ95H12 may be used together with a LZ93J21, a V40 and optionally, a 8087,

The LZ95H12 incorporates the following functions:

1. V40/system address bus interfacing;
2. V40/system data bus interfacing;
3. V40 oscillator selection;
4. bus cycle generator and IO channel interface:
5. 8087 interface;
6. system ROM interface;
7. DRAM control signal generation;
8. system timer clock generation;
9. speaker control;
10. keyboard interface;
11. configuration switch port;
12. NMI control and IO trapping;
13. SCM interface; and
14. internal I/O register interface.

LZ95H12 Block Diagram



LZ95H12

No.	Signal name	I/O	Description
1	$\overline{WE1}$	O	Not used
2	$\overline{OE0}$	O	DRAM output enable
3	$\overline{OE1}$	O	Not used
4	RESET	I	System reset signal inut
5	$\overline{ROMCE}$	O	ROM chip enable
6	$\overline{ROMOE}$	O	ROM output enable
7	BS0	I	Bus status 0
8	BS1	I	Bus status 1
9	BS2	I	Bus status 2
10	AD0	I/O	AD bus 0
11	AD1	I/O	AD bus 1
12	AD2	I/O	AD bus 2
13	AD3	I/O	AD bus 3
14	AD4	I/O	AD bus 4
15	AD5	I/O	AD bus 5
16	Vcc		
17	GND		
18	AD6	I/O	AD bus 6
19	AD7	I/O	AD bus 7
20	A8	I	CPU address 8
21	A9	I	CPU address 9
22	A10	I	CPU address 10
23	A11	I	CPU address 11
24	A12	I	CPU address 12
25	A13	I	CPU address 13
26	A14	I	CPU address 14
27	A15	I	CPU address 15
28	A16	I	CPU address 16
29	A17	I	CPU address 17
30	A18	I	CPU address 18
31	A19	I	CPU address 19
32	RDY87	O	Ready signal for 8087
33	RDYV40	O	Ready signal for V40
34	$\overline{REFRQ}$	I	Refresh request
35	$\overline{RQ/GT0}$	I/O	Request/Grant 0
36	IRQ87	I	Interrupt request from 8087
37	HLDAK	I	Bus hold acknowledge
38	HLDRQ	O	Bus hold request
39	TCLK	O	Timer clock
40	TCTL2	O	Timer 2 control
41	TOUT2	I	Timer 2 output
42	IRQ1	O	Interrupt 1
43	NMI	O	Non-maskable interrupt
44	$\overline{TC}$	I	Terminal count
45	CPUCLK	I	CPU clock
46	X1	O	Connected with X1 pin of V40
47	CPOSC0	O	Connected with 20MHz crystal
48	CPOSC1	I	
49	GND		
50	Vcc		
51	VOSC	O	Clock output for LZ93J21
52	OSC0	O	Connected with 14.31818MHz crystal
53	OSC1	I	
54	AEN	I	DMA or refresh active signal
55	$\overline{EXTM}$	I/O	External memory active signal

No.	Signal name	I/O	Description
56	EXTIO	I/O	External I/O active signal
57	SLOCYC	I	Signal to decide bus cycle
58	EXPDIR	O	Not used
59	EXPBEN	O	Not used
60	IOCHK	I	Not used
61	READY	I	Ready
62	STC	O	Terminal count output
63	SYSCLK	O	System clock
64	ALE	O	Address latch enable
65	SD0	I/O	System data bus 0
66	SD1	I/O	System data bus 1
67	SD2	I/O	System data bus 2
68	SD3	I/O	System data bus 3
69	SD4	I/O	System data bus 4
70	SD5	I/O	System data bus 5
71	SD6	I/O	System data bus 6
72	SD7	I/O	System data bus 7
73	SA0	O	System address bus 0
74	SA1	O	System address bus 1
75	SA2	O	System address bus 2
76	SA3	O	System address bus 3
77	SA4	O	System address bus 4
78	SA5	O	System address bus 5
79	SA6	O	System address bus 6
80	Vcc		
81	GND		
82	SA7	O	System address bus 7
83	SA8	O	System address bus 8
84	SA9	O	System address bus 9
85	SA10	O	System address bus 10
86	SA11	O	System address bus 11
87	SA12	O	System address bus 12
88	SA13	O	System address bus 13
89	GND		
90	SA14	O	System address bus 14
91	SA15	O	System address bus 15
92	SA16	O	System address bus 16
93	SA17	O	System address bus 17
94	SA18	O	System address bus 18
95	SA19	O	System address bus 19
96	$\overline{\text{SMRD}}$	O	System memory read
97	$\overline{\text{SMWR}}$	O	System memory write
98	$\overline{\text{SIORD}}$	O	System I/O rend
99	$\overline{\text{SIOWR}}$	O	System I/O write
100	SPEAKR	O	Speaker signal
101	KCLK	I/O	Key clock
102	KDATA	I/O	Key data
103	CPUHS	O	Signal for handshake CPU-SCM
104	SCMHS	I	Signal for handshake CPU-SCM
105	IPC0	I/O	IPC bus 0
106	IPC1	I/O	IPC bus 1
107	IPC2	I/O	IPC bus 2
108	IPC3	I/O	IPC bus 3
109	MA0	O	Multiplexed DRAM address 0
110	MA1	O	Multiplexed DRAM address 1
111	MA2	O	Multiplexed DRAM address 2
112	Vcc		

No.	Signal name	I/O	Description
113	GND		
114	MA3	O	Multiplexed DRAM address 3
115	MA4	O	Multiplexed DRAM address 4
116	MA5	O	Multiplexed DRAM address 5
117	MA6	O	Multiplexed DRAM address 6
118	MA7	O	Multiplexed DRAM address 7
119	MA8	O	Multiplexed DRAM address 8
120	GND		
121	$\overline{\text{RAS0}}$	O	DRAM-RAS output
122	$\overline{\text{RAS1}}$	O	DRAM-RAS output
123	$\overline{\text{CAS0}}$	O	DRAM-CAS output
124	$\overline{\text{CAS1}}$	O	DRAM-CAS output
125	$\overline{\text{CAS2}}$	O	DRAM-CAS output
126	$\overline{\text{CAS3}}$	O	DRAM-CAS output
127	$\overline{\text{CAS4}}$	O	DRAM-CAS output
128	$\overline{\text{WE0}}$	O	DRAM write enable

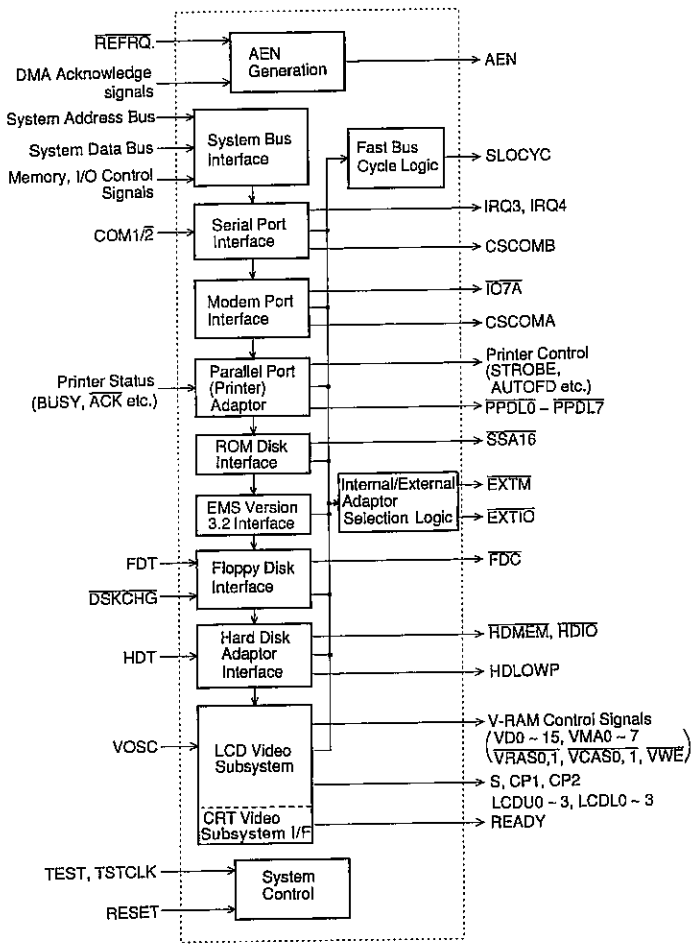
7-7. LZ93J21 (Gate array)

General

The LZ93J21 may be used together with a LZ95H12, a V40 and optionally. The LZ93J21 incorporates the following functions:

1. system bus interface;
2. AEN generation;
3. serial port interface;
4. modem port interface;
5. parallel port adapter;
6. ROM disk interface;
7. EMS Version 3.2 interface;
8. floppy disk adapter extension;
9. hard disk adapter interface;
10. CRT video subsystem interface;
11. LCD video subsystem;
12. fast bus cycle logic; and
13. internal/external adapter selection logic.

LZ93J21 Block Diagram



LZ93J21 signal description

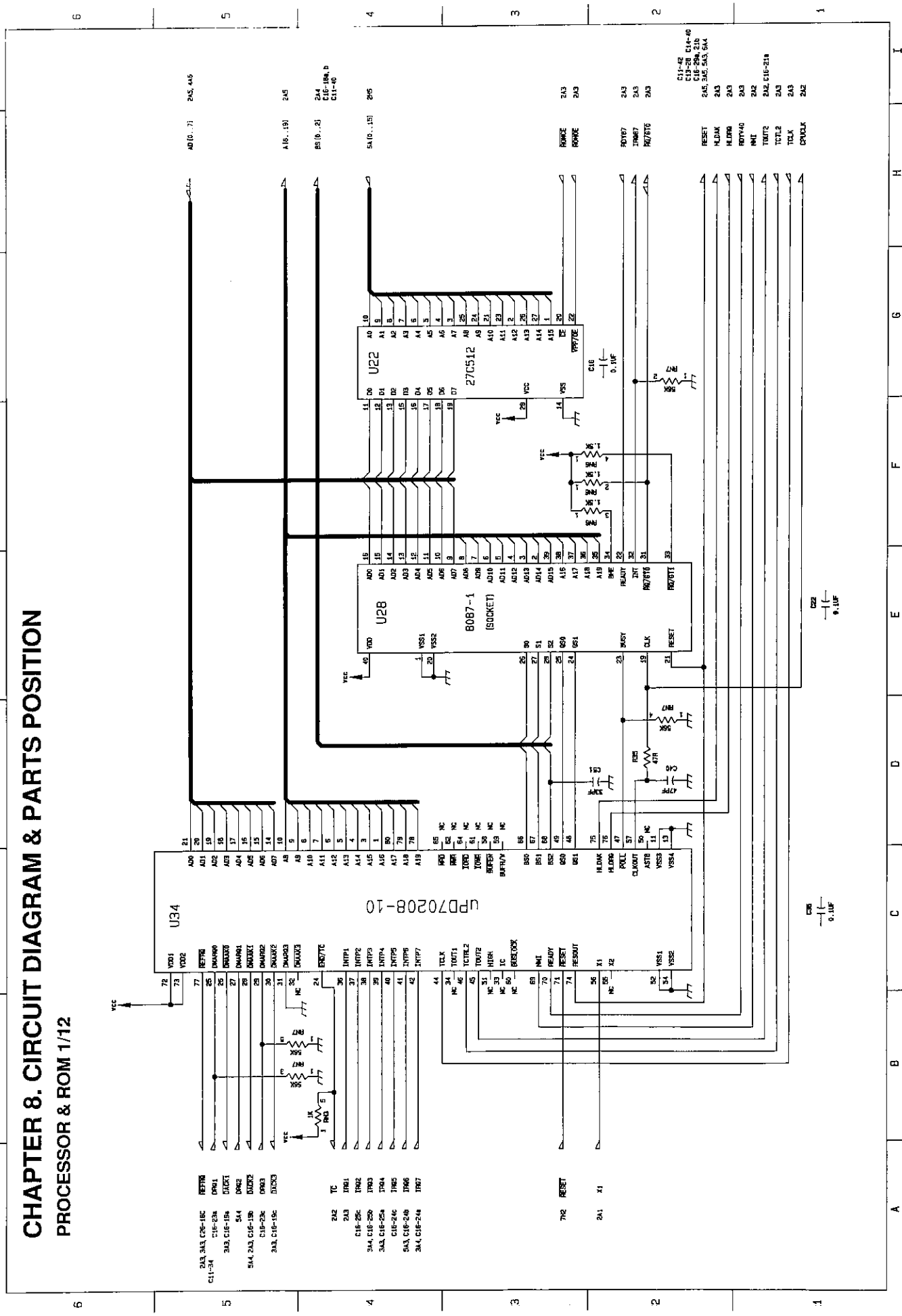
No.	Signal name	I/O	Description
1	$\overline{\text{DACK1}}$	I	Input to V40 channel 0 DMA acknowledge
2	$\overline{\text{DACK2}}$	I	Input to V40 channel 1 DMA acknowledge
3	$\overline{\text{DACK3}}$	I	Input to V40 channel 2 DMA acknowledge
4	$\overline{\text{SMRD}}$	I	Input to active low memory read signal
5	$\overline{\text{SMWR}}$	I	Input to active low memory write signal
6	$\overline{\text{SIORD}}$	I	Input to active low I/O read signal
7	$\overline{\text{SIOWR}}$	I	Input to active low I/O write signal
8	VD0	I/O	LCD VRAM data bus 0
9	VD1	I/O	LCD VRAM data bus 1
10	VD2	I/O	LCD VRAM data bus 2
11	VD3	I/O	LCD VRAM data bus 3
12	VD4	I/O	LCD VRAM data bus 4
13	VD5	I/O	LCD VRAM data bus 5
14	VD6	I/O	LCD VRAM data bus 6
15	VD7	I/O	LCD VRAM data bus 7
16	Vcc		+5V supply
17	GND		0V, ground
18	VD8	I/O	LCD VRAM data bus 8
19	VD9	I/O	LCD VRAM data bus 9
20	VD10	I/O	LCD VRAM data bus 10
21	VD11	I/O	LCD VRAM data bus 11
22	VD12	I/O	LCD VRAM data bus 12
23	VD13	I/O	LCD VRAM data bus 13
24	VD14	I/O	LCD VRAM data bus 14
25	VD15	I/O	LCD VRAM data bus 15
26	VMA0	O	LCD VRAM address bus 0
27	VMA1	O	LCD VRAM address bus 1
28	VMA2	O	LCD VRAM address bus 2
29	VMA3	O	LCD VRAM address bus 3
30	VMA4	O	LCD VRAM address bus 4
31	VMA5	O	LCD VRAM address bus 5
32	VMA6	O	LCD VRAM address bus 6
33	VMA7	O	LCD VRAM address bus 7
34	TEST	I	Test pin
35	$\overline{\text{VRAS0}}$	O	LCD VRAM 0 row address select signal (active low)
36	$\overline{\text{VRAS1}}$	O	LCD VRAM 1 row address select signal (active low)
37	$\overline{\text{VCAS0}}$	O	LCD VRAM 0 column address select signal (active low)
38	$\overline{\text{VCAS1}}$	O	LCD VRAM 1 column address select signal (active low)
39	$\overline{\text{VWE}}$	O	LCD VRAM write enable signal (active low)
40	$\overline{\text{HDMEM}}$	O	Hard disk memory select signal (active low)
41	$\overline{\text{HDIO}}$	O	Hard disk I/O select signal (active low)
42	$\overline{\text{SSA16}}$	O	EMS memory card system address bus 16
43	HDLOWP	O	Not used
44	HDT	I	1: HD 0: FD
45	FDT	I	LOW.
46	READY	O	Bus cycle ready signal
47	SLOCYC	O	Slow bus cycle select signal
48	RESET	I	Reset signal input (active high)
49	GND		
50	Vcc		
51	IRQ3	O	V40 channel 3 interrupt request signal
52	IRQ4	O	V40 channel 4 interrupt request signal

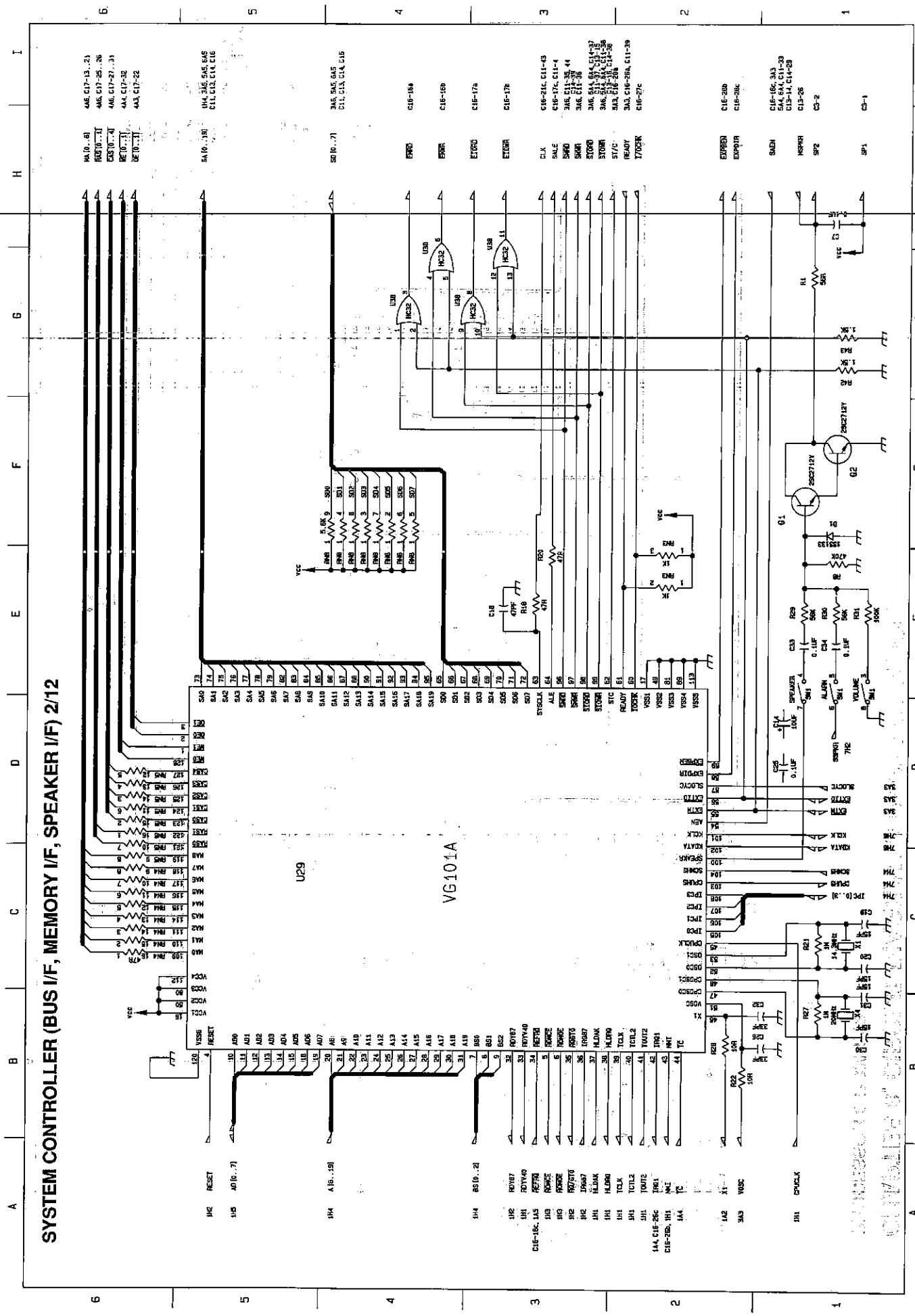
No.	Signal name	I/O	Description
53	IRQ7	O	V40 channel 7 interrupt request signal
54	EXTM	O	External memory active signal (active low)
55	EXTIO	O	External I/O active signal (active low)
56	FDC	O	Floppy disk controller select signal (active low)
57	DSKCHG	I	Input to disk change signal (active low)
58	HID	O	(active low)
59	IO7A	O	7AH I/O port select signal (active low)
60	CSCOMA	O	COMA chip select signal (active high)
61	SIRQ	I	Input to 82C50 interrupt request signal
62	SINTEN	I	Input to 82C50 interrupt enable signal
63	CSCOMB	O	COMB chip select signal (active high)
64	COM1/2	I	Input to COM 1, COM 2 select signal from the sub-CPU
65	BUSY	I	Input to printer busy signal
66	ACK	I	Input to printer acknowledge signal
67	PE	I	Input to printer paper empty signal
68	SELECT	I	Input to printer select signal
69	ERROR	I	Input to printer error signal
70	SEL	O	Printer select signal
71	INIT	O	Printer initialize signal
72	AUTOFD	O	Printer linefeed enable signal
73	STROBE	O	Printer strobe signal
74	PPDL0	O	Data output 0 to printer
75	PPDL1	O	Data output 1 to printer
76	PPDL2	O	Data output 2 to printer
77	PPDL3	O	Data output 3 to printer
78	PPDL4	O	Data output 4 to printer
79	PPDL5	O	Data output 5 to printer
80	Vcc		+5V supply
81	GND		0V, ground
82	PPDL6	O	Data output 6 to printer
83	PPDL7	O	Data output 7 to printer
84	TSTCLK	I	Test clock input
85	S	O	LCD scan start signal
86	CP1	O	LCD data latch signal
87	CP2	O	LCD data shift clock
88	LCDU0	O	Upper row LCD data 0
89	LCDU1	O	Upper row LCD data 1
90	LCDU2	O	Upper row LCD data 2
91	LCDU3	O	Upper row LCD data 3
92	LCDL0	O	Lower row LCD data 0
93	LCDL1	O	Lower row LCD data 1
94	LCDL2	O	Lower row LCD data 2
95	LCDL3	O	Lower row LCD data 3
96	VOSC	I	LCD controller clock input
97	SD0	I/O	System data bus 0
98	SD1	I/O	System data bus 1
99	SD2	I/O	System data bus 2
100	SD3	I/O	System data bus 3
101	SD4	I/O	System data bus 4
102	SD5	I/O	System data bus 5
103	SD6	I/O	System data bus 6
104	SD7	I/O	System data bus 7
105	SA0	I	System address bus 0
106	SA1	I	System address bus 1
107	SA2	I	System address bus 2

No.	Signal name	I/O	Description
108	SA3	I	System address bus 3
109	SA4	I	System address bus 4
110	SA5	I	System address bus 5
111	SA6	I	System address bus 6
112	Vcc		+5V supply
113	GND		0V, ground
114	SA7	I	System address bus 7
115	SA8	I	System address bus 8
116	SA9	I	System address bus 9
117	SA10	I	System address bus 10
118	SA11	I	System address bus 11
119	SA12	I	System address bus 12
120	SA13	I	System address bus 13
121	SA14	I	System address bus 14
122	SA15	I	System address bus 15
123	SA16	I	System address bus 16
124	SA17	I	System address bus 17
125	SA18	I	System address bus 18
126	SA19	I	System address bus 19
127	AEN	O	DMA refresh active signal
128	REFRQ	I	Input to refresh request signal from V40

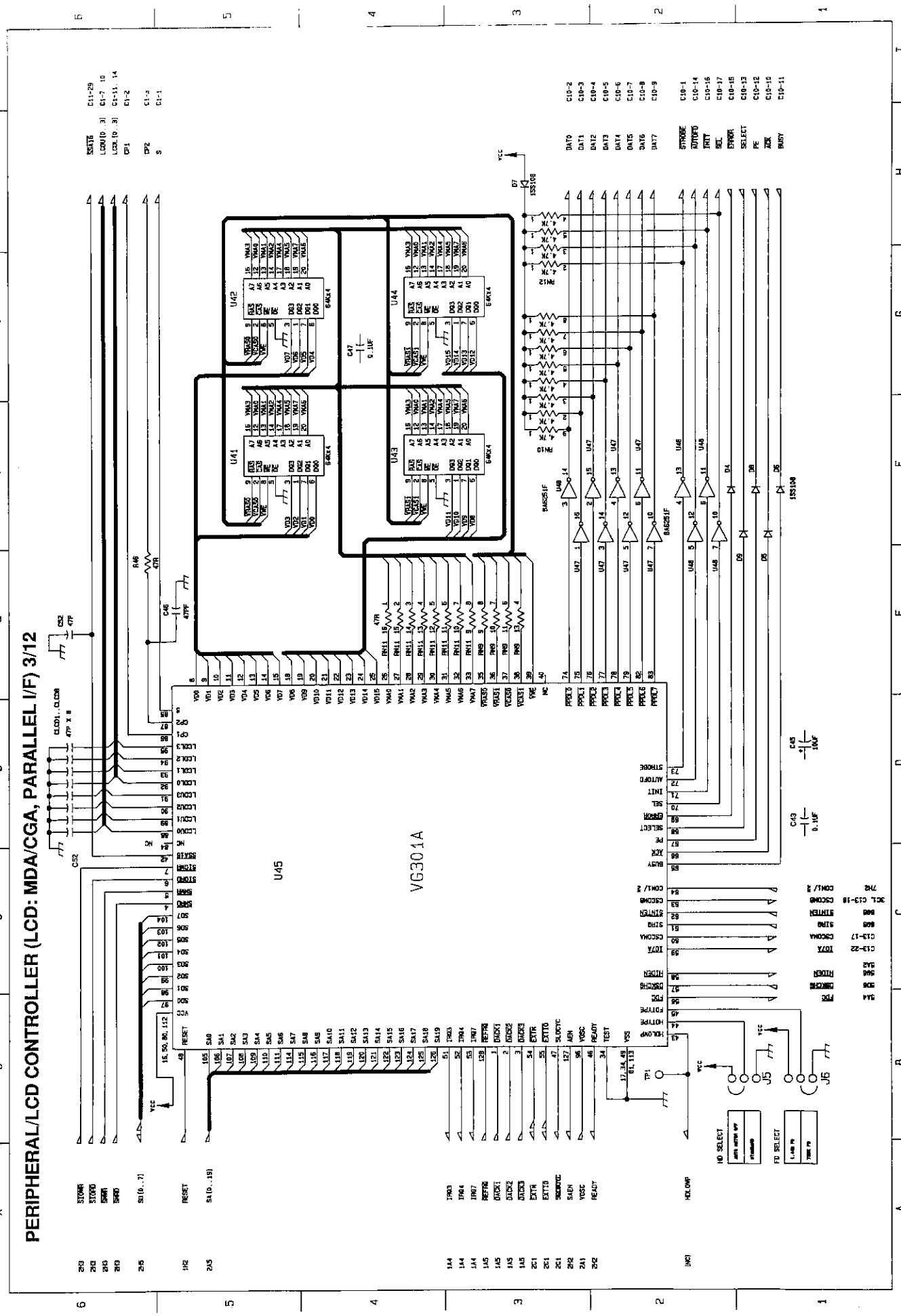
CHAPTER 8. CIRCUIT DIAGRAM & PARTS POSITION

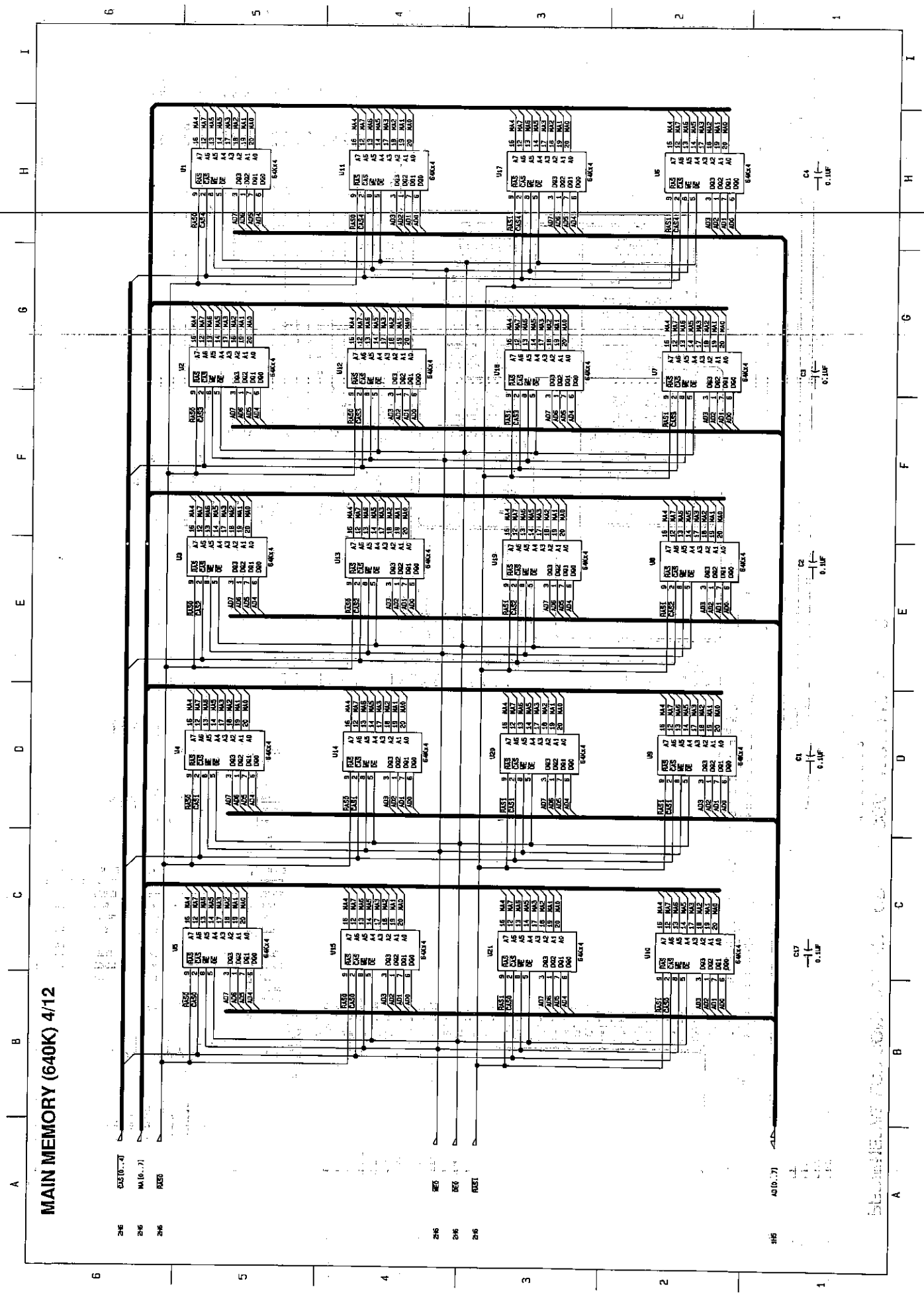
PROCESSOR & ROM 1/12



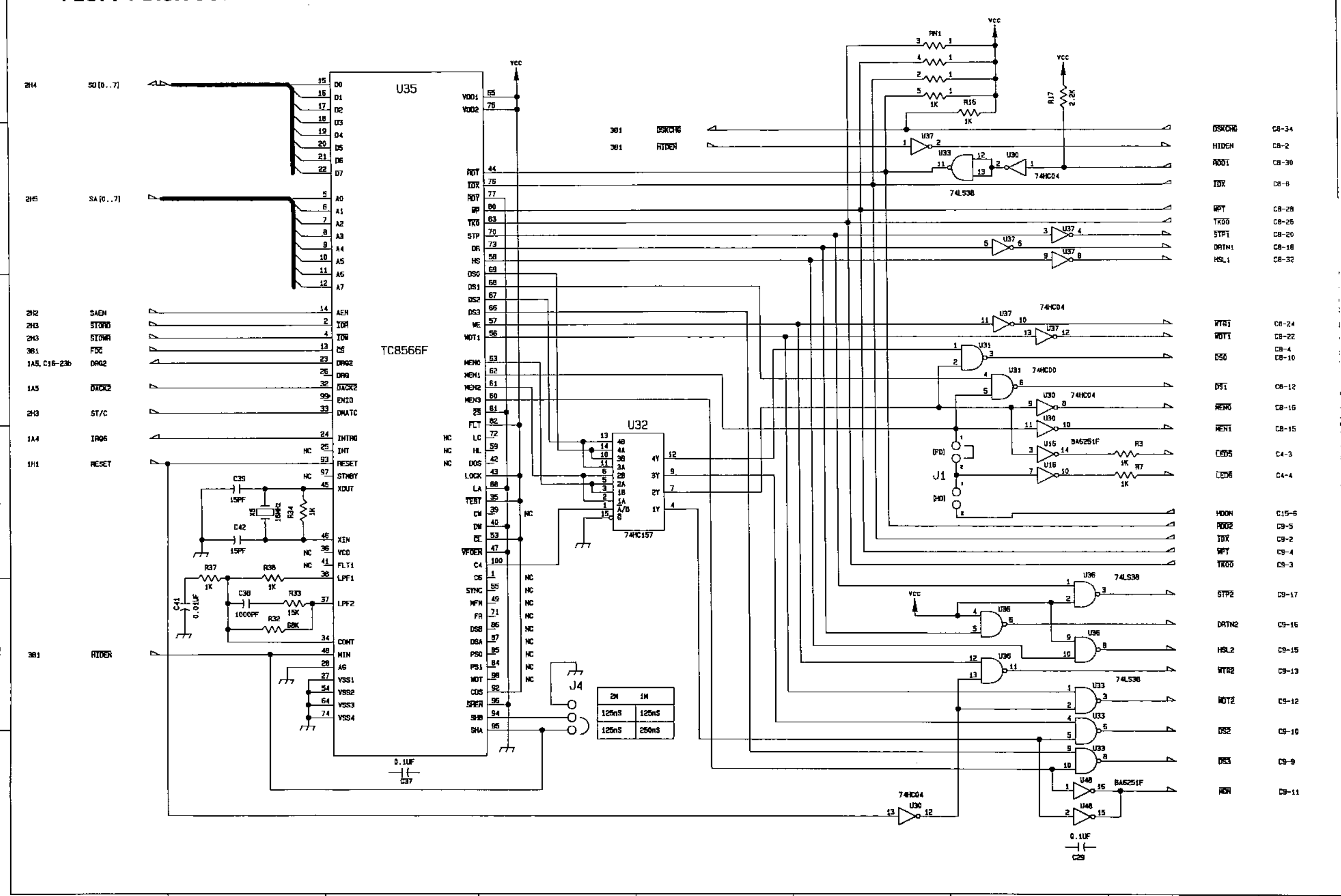

SYSTEM CONTROLLER (BUS I/F, MEMORY I/F, SPEAKER I/F) 2/12
VG101A
U29

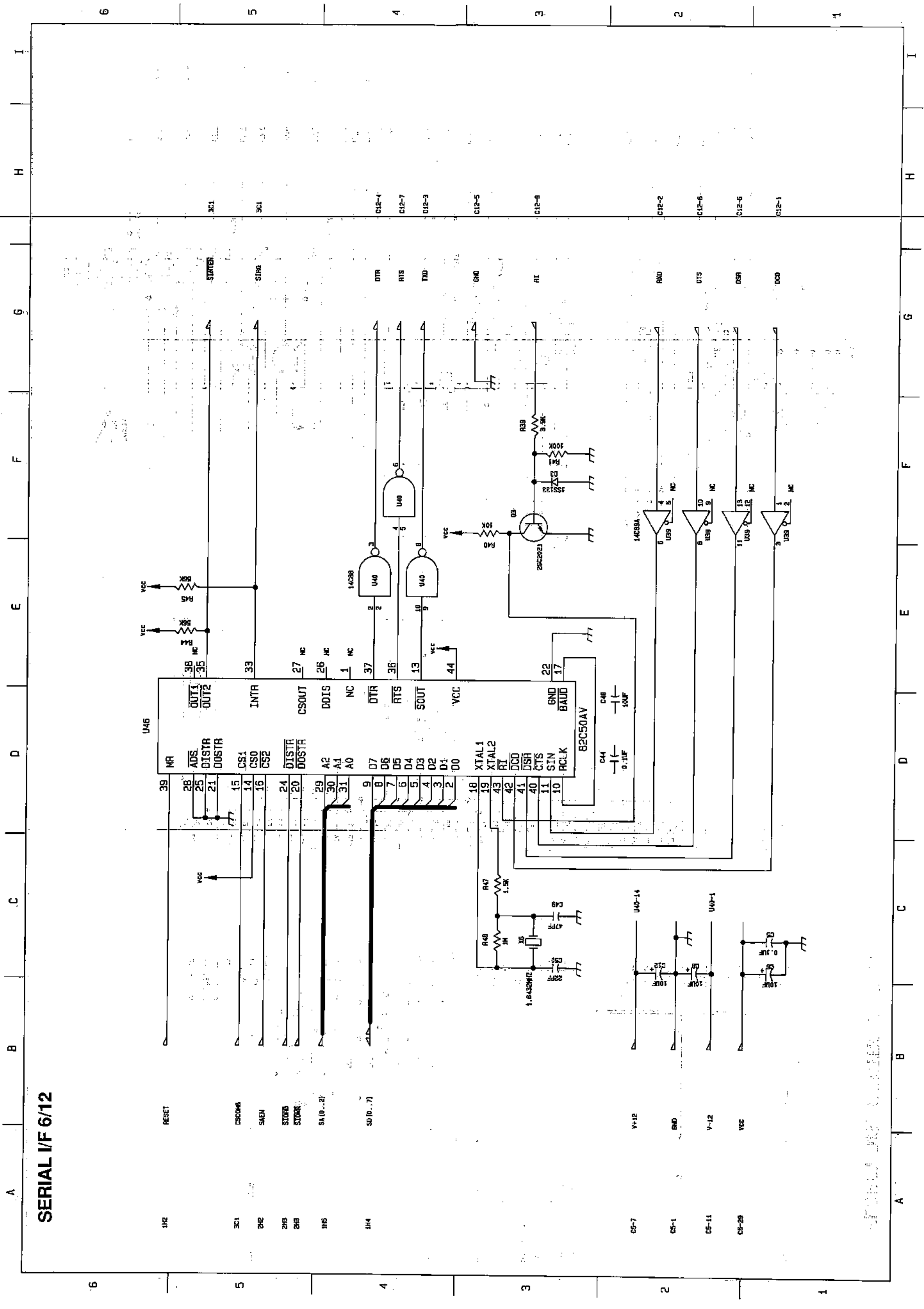
PERIPHERAL/LCD CONTROLLER (LCD: MDA/CGA, PARALLEL I/F) 3/12



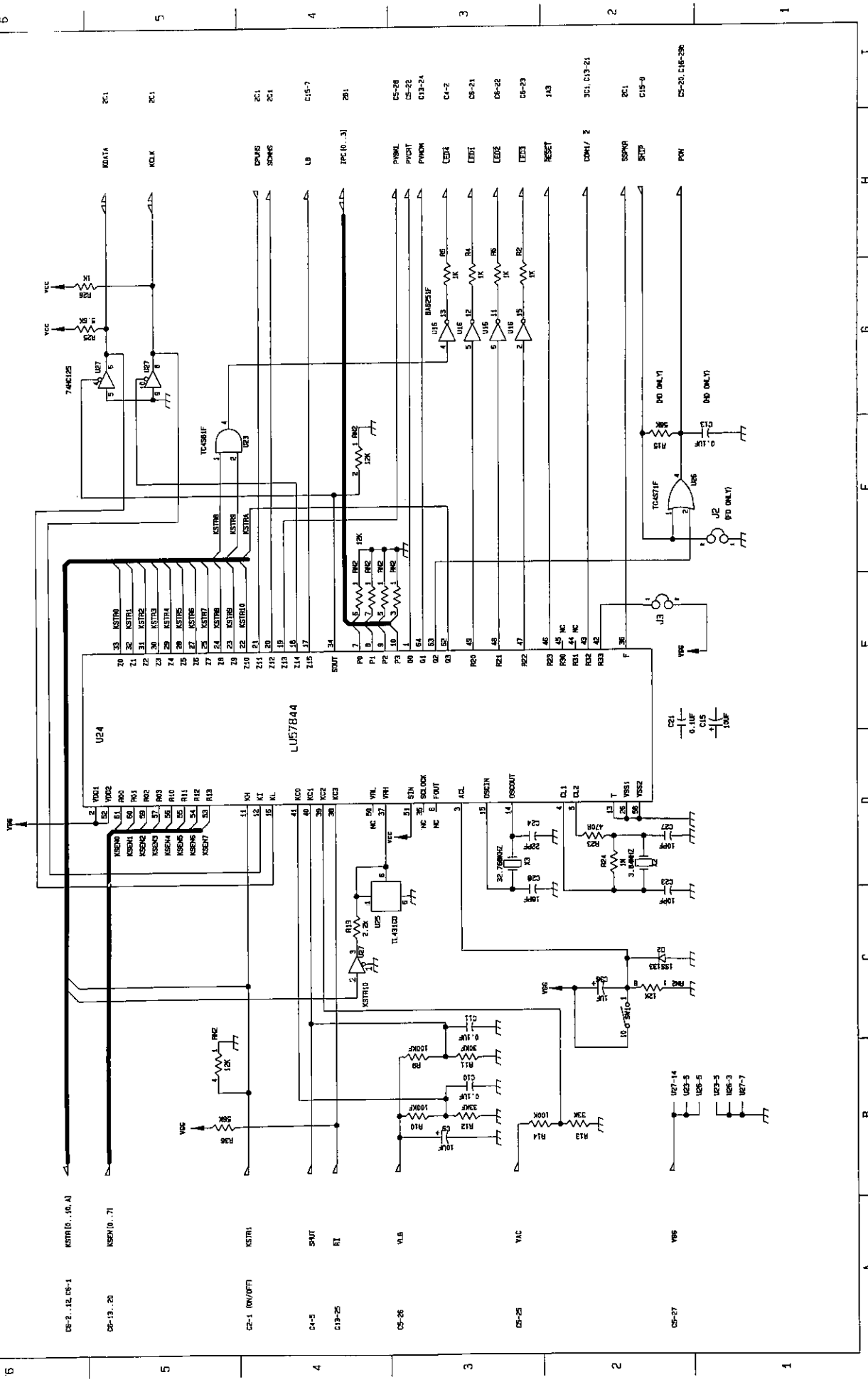

MAIN MEMORY (640K) 4/12

FLOPPY DISK CONTROLLER & I/F 5/12

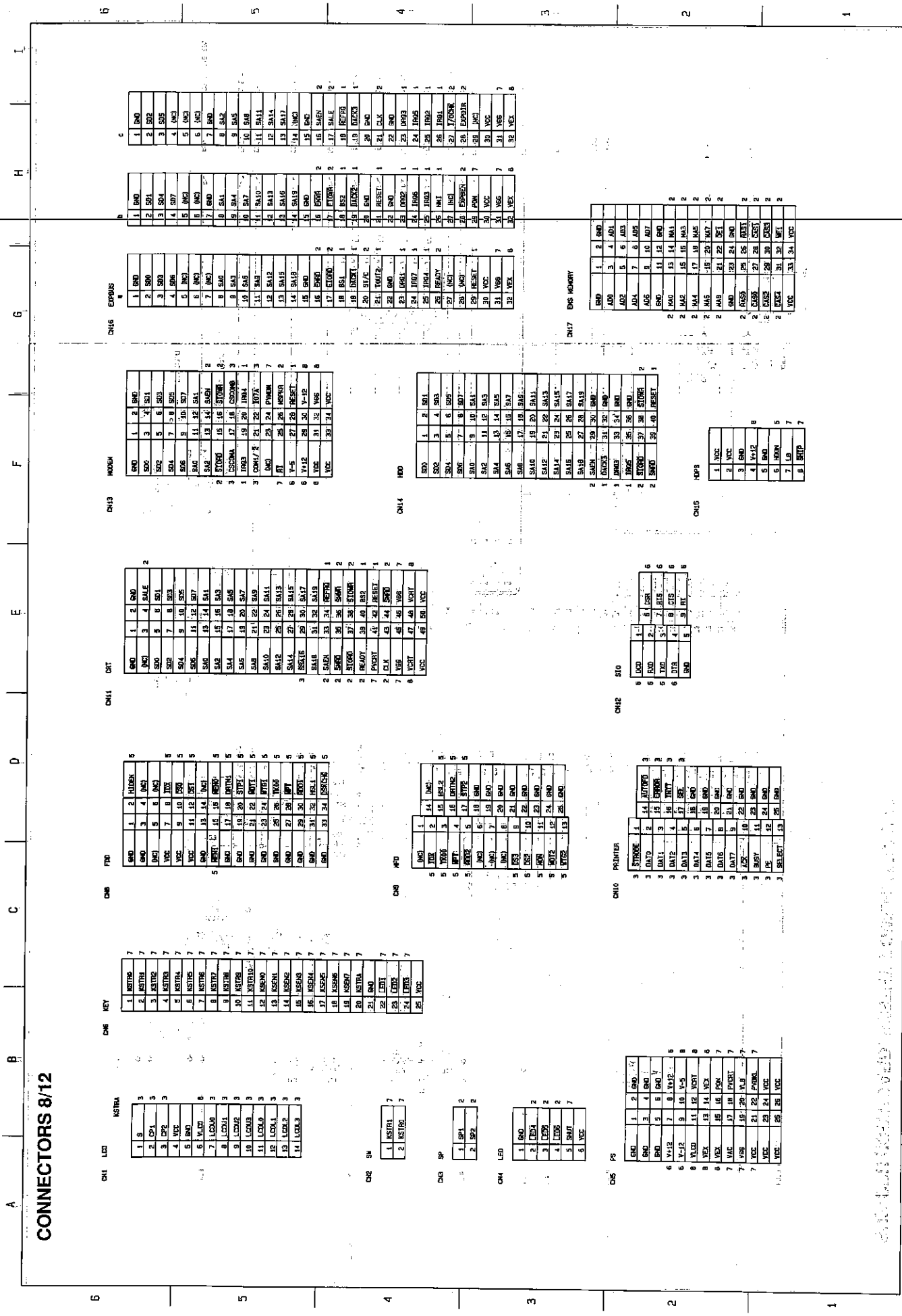



SERIAL I/F 6/12
U46
82C50AV
MR
ADS
DISTR
DOSTR
CS1
CS0
CS2
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
XTAL1
XTAL2
RI
DCD
DSR
CTS
SIN
RCLK
OUT1
OUT2
INTR
CSOUT
DDIS
NC
DTR
RTS
SOUT
VCC
GND
BAUD
U40
U39
14C88
14C89A
2SC2021
1S2222
RESET
CSCOMB
SAEN
SIORD
SIOWR
SA[0..2]
SD[0..7]
V+12
GND
V-12
VCC
DTR
RTS
TXD
GND
RI
RXD
CTS
DSR
DCD
1.8432MHZ

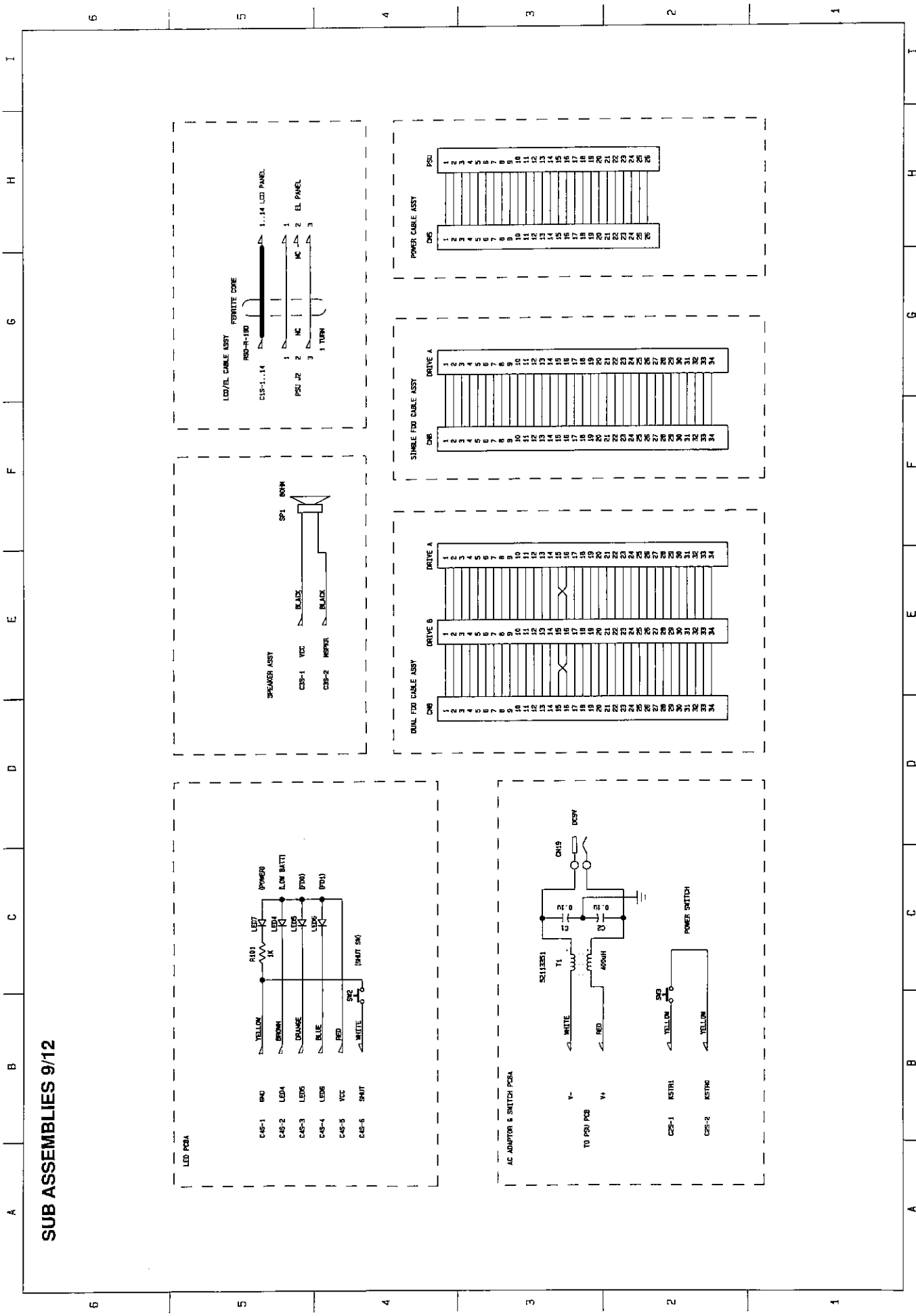
SUB-CPU (KEYBOARD, SYSTEM POWER, RTC) 7/12



CONNECTORS 8/12

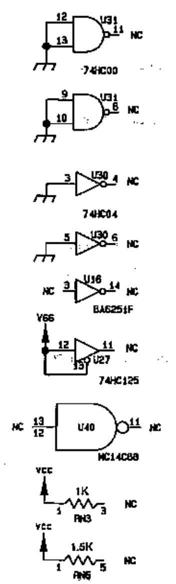


SUB ASSEMBLIES 9/12



10/12

SPARE GATES



DESIGNATORS

LAST USE	NOT USED
C50	
CN17	CN7
D9	
J6	
R48	
RN12	
U3	
U48	
X6	

RAM CHIPS

START	LAST ADDRESS	BIT 7-4	BIT 3-0
000K	00FFFF	U5	U15
64K	01FFFF	U21	U10
128K	02FFFF	U4	U14
192K	03FFFF	U20	U9
256K	04FFFF	U3	U13
320K	05FFFF	U19	U8
384K	06FFFF	U2	U12
448K	07FFFF	U18	U7
512K	08FFFF	U1	U11
576K	09FFFF	U17	U6

DIP SWITCH

SW1	ON	OFF
1	RESET SUB-CPU	NORMAL OPERATION
2	NORMAL	SPARE
3	SPEAKER LOW VOLUME	NORMAL
4	NORMAL	PC SPEAKER OFF
5	NORMAL	LOW BATT/SHUT ALARM OFF

JUMPER

LOCATION	FUNCTION	NORMAL SETTING	SPECIAL SETTING
J1	SELECT LED INDICATOR SOURCE	DUAL FDD - FD HDD/FDD - HD	
J2	SUPPRESS SHIP SIGNAL WHEN NO HDD IS INSTALLED	DUAL FDD - O HDD/FDD - X	
J3	SELECT KEYBOARD SIZE	WITH 10 KEY	(CUT TRACE) W/O 10 KEY
J4	FDD WRITE PRE-COMP PERIOD (720K)	250nS	(CUT & JMP) 125NS
J5	HDD MOTOR CONTROL	ALWAYS ON	(CUT & JMP) AUTO POWER OFF
J6	FDD TYPE SELECT	720K	(CUT & JMP) 1.44M

DUAL FDD PCBA VS SINGLE FDD/HDD PCBA

ITEM	DUAL FDD VERSION	HDD/FDD VERSION
R9	97.6KF	100KF
R15	NIL	56K
C13	NIL	0.1uF
J3	FD SIDE	HD SIDE
J2	INSTALL	NIL
CN14	NIL	INSTALL
CN15	NIL	INSTALL
J5	NIL	CUT & JMP

ECN FOR REV2 PCB — 10-12-1988

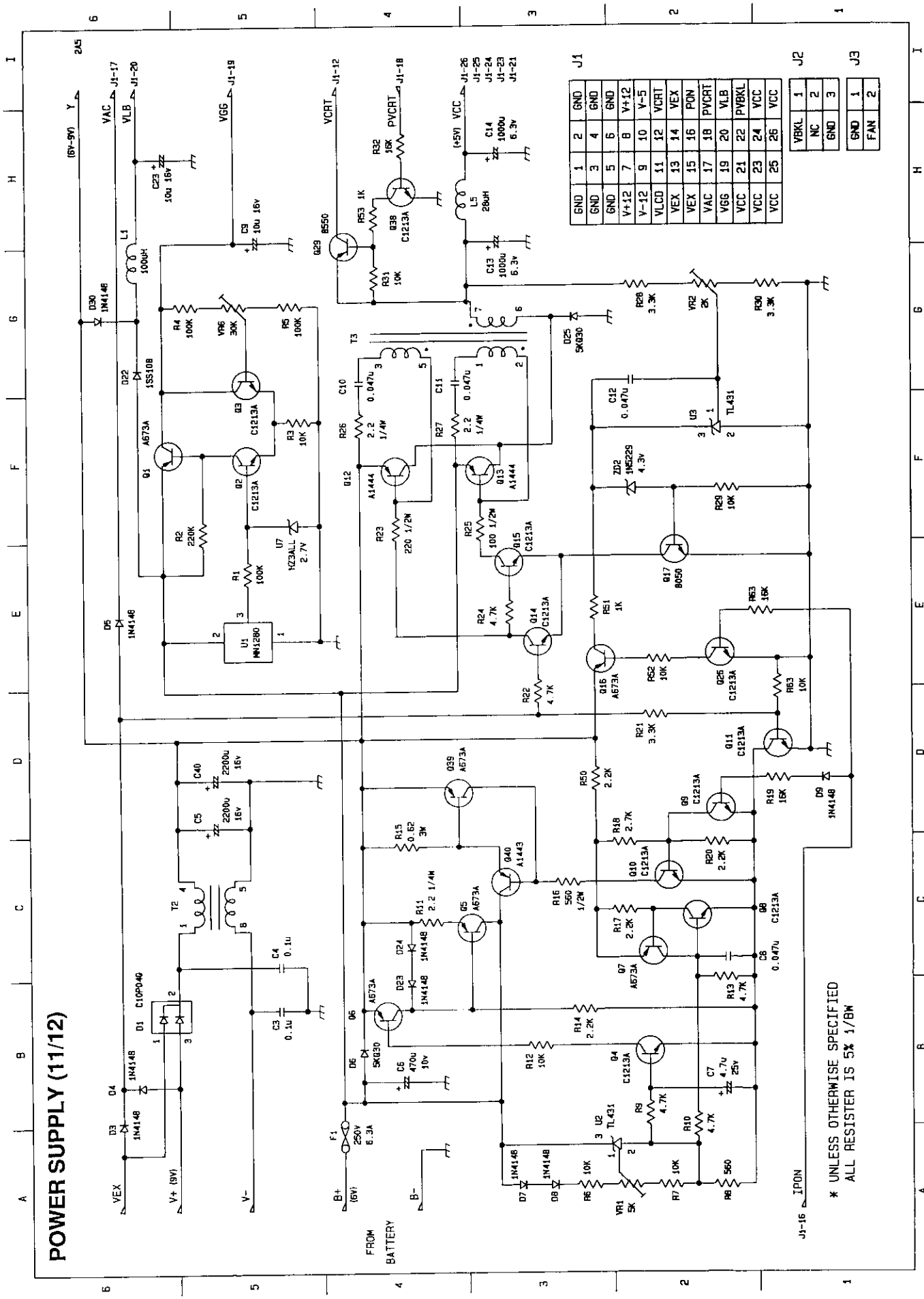
1. SWAP PIN 1 AND PIN 2 OF U27 (74HC125).
2. CONNECT PIN 92 OF U34 (TC8566F) TO VCC.
3. ENLARGE ANGLE BRACKET PAD ON COMP. SIDE BY 0.5MM ON EACH SIDE.
4. ATTACH ON SOLDER SIDE, CLCD1..8 (47PF) TO CN1-7..14

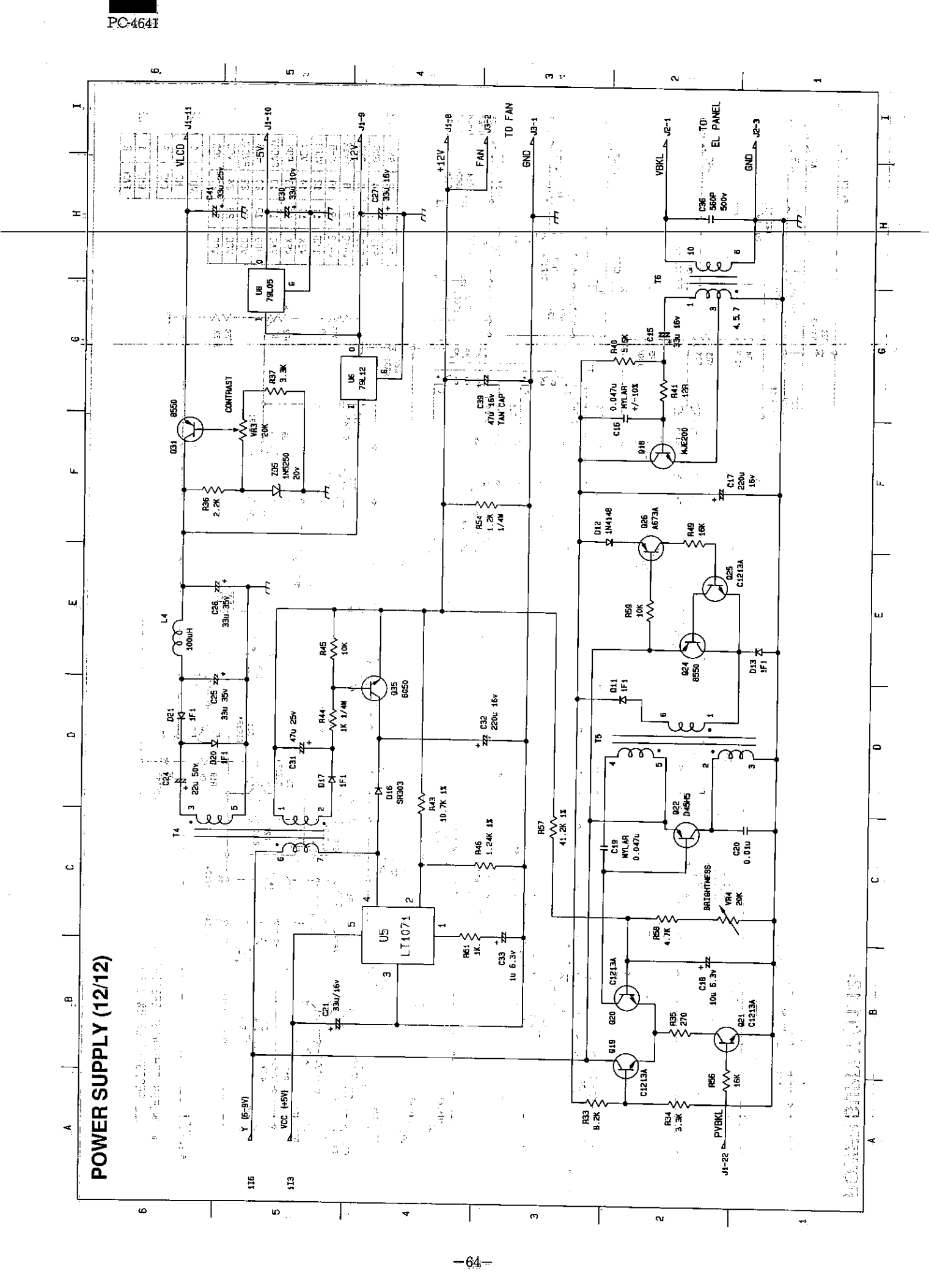
ECN FOR REV2B PCB — 10-12-1988

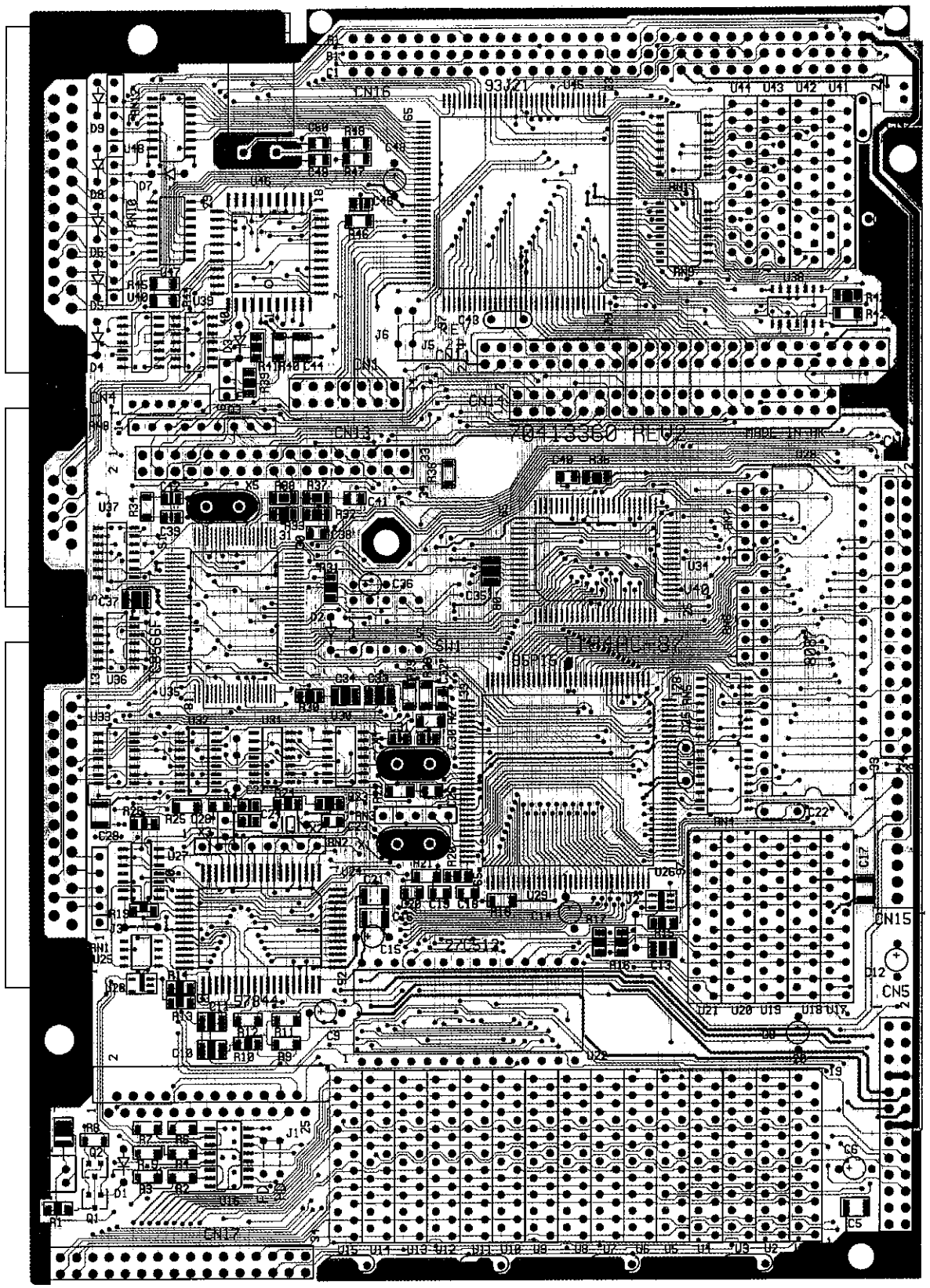
1. ENLARGE ANGLE BRACKET PAD ON COMP. SIDE BY 0.5MM ON EACH SIDE.
2. ATTACH ON SOLDER SIDE, COLO1..8 (47PF) TO CN1-7..14

ECN FOR REV3 PCB — 11-8-1988

1. ATTACH ON SOLDER SIDE, CLCD1..8 (47PF) TO CN1-7..14

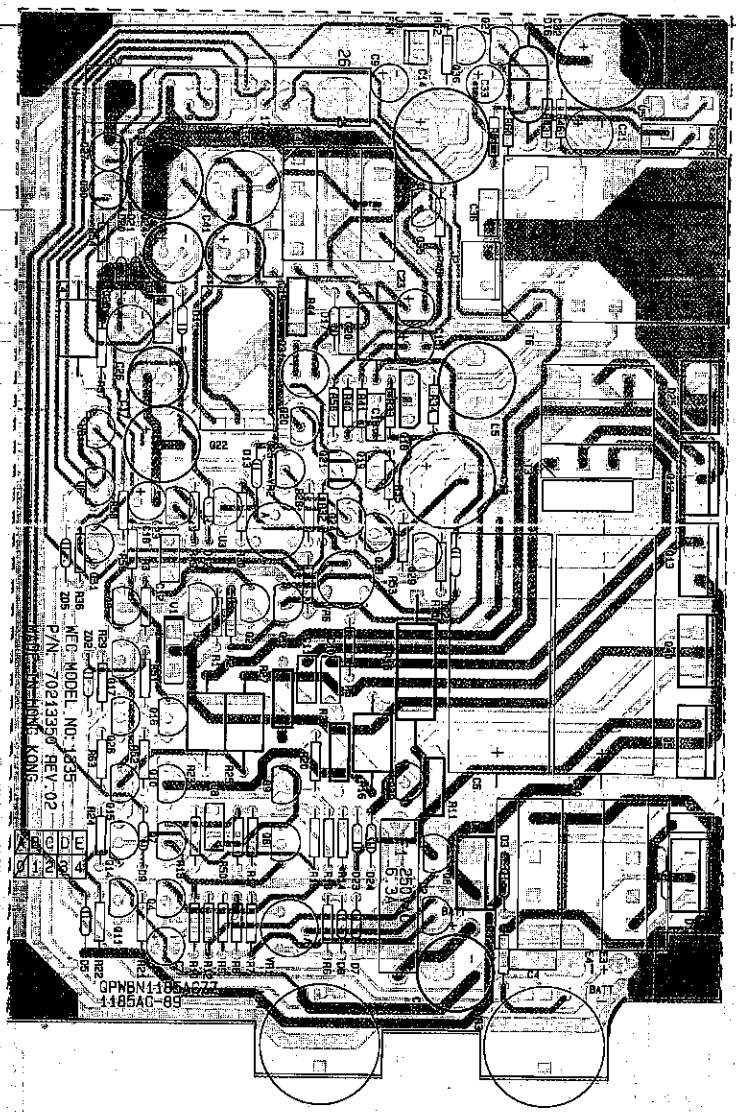

POWER SUPPLY (11/12)
J1
J2
J3
VBKL
NC
GND
FAN
* UNLESS OTHERWISE SPECIFIED
ALL RESISTER IS 5% 1/8W
FROM BATTERY
VEX
V+ (9V)
V-
B+ (6V)
B-
IPON
VAC
VLB
VGG
VCRT
PVCRT
VCC
(+5V)
(6V-9V)


POWER SUPPLY (12/12)
VLCD
-5V
12V
+12V
FAN
TO FAN
GND
VBKL
TO EL PANEL
GND
CONTRAST
BRIGHTNESS
U8 79L05
U6 79L12
U5 LT1071
T4
T5
T6
L4 100uH
Y (6-9V)
VCC (+5V)
PVBKL

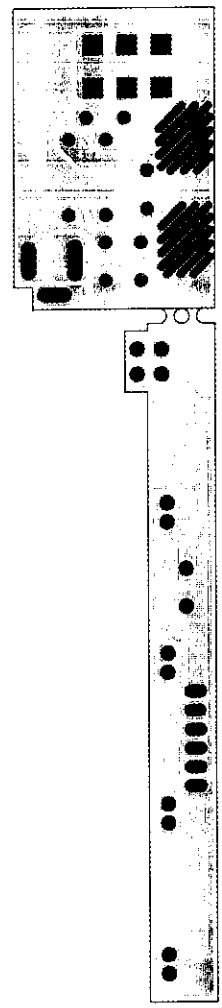


MAIN P.W.B.

POWER CIRCUIT PARTS LAYOUT



LED P.W.B. & SWITCH P.W.B.



LED P.W.B. & SWITCH P.W.B.

SHARP PARTS GUIDE

PC-4602
MODEL PC-4641

CONTENTS

DESTINATION TABLE

U	USA	E	EJ	Korea
Y	Canada		ESC	Venezela
G	Germany, Austria		ESCI	Taiwan
H	U.Kingdom		EQ	New Zealand
Q	Australia		EH	Malaysia
K	Hong Kong		ESG	Indonesia
S	Singapore		ISGI	Philippines
W	Switzerland (Germany)		ESB	Saudi Arabia

DEFINITION

The definition of each Rank is as follows and also noted in the list

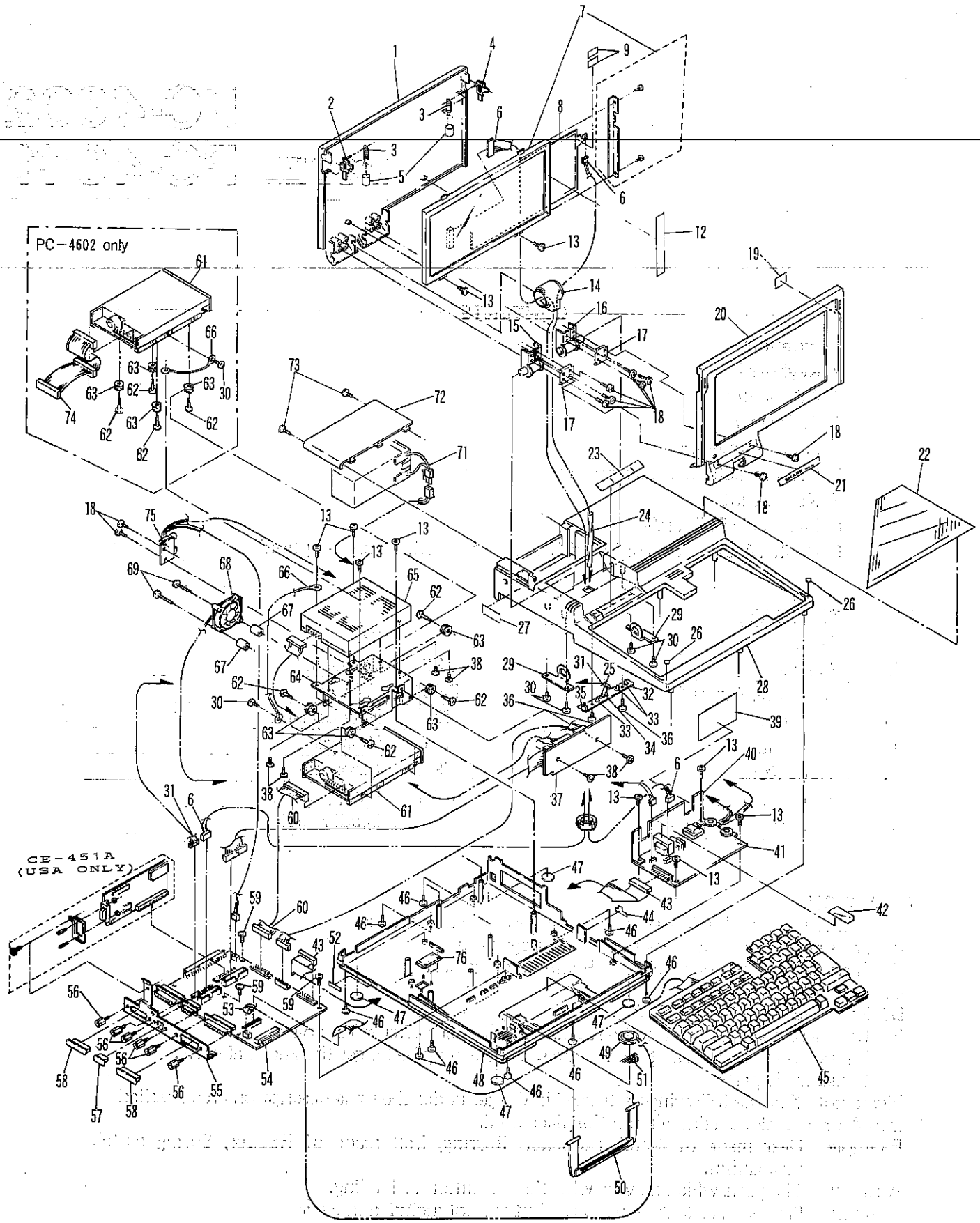
A: Parts necessary to be stocked as High usage parts.
B: Parts necessary to be stocked as Standard usage parts.
C: Low usage parts.
D: Parts necessary for refurbish.
E: Unit parts recommended to be stocked for efficient after sales service.
Please note that the lead time for the said parts may be longer than normal parts.
S: Consumable parts.

Please note that the following parts used in Copier under the same description are classified into A or B Rank depending upon the place used.

Example: Gear made of Metal, Sprocket, Bearing, Belt made of Rubber, Spring clutch mechanism.
A Rank: The parts which may be with the revolution or loading.
B Rank: Parts similar to A Rank parts, but are not included in Rank A.

Parts marked with "⚠" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

1 Exteriors



1 Exteriors

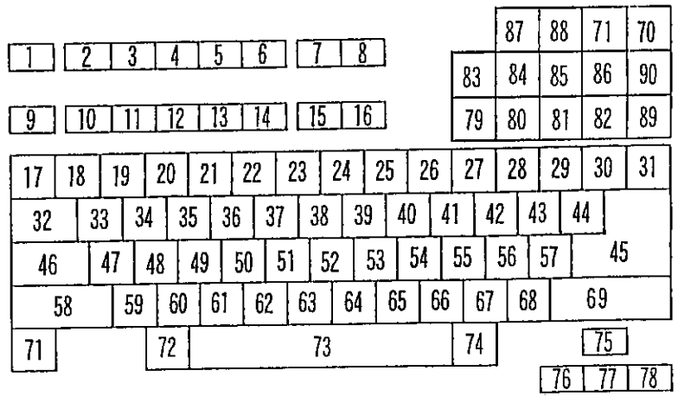
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	0GM731336 03//	BA	N	D	CAB−C/White	(G,W)
	0GM731336 13//	BA	N	D	CAB−C/Black	(U,Y,H,Q,K,S,E)
2	0GM731336 06//	AC	N	C	Hook (L)/White	(G,W)
	0GM731336 16//	AC	N	C	Hook (L)/Black	(U,Y,H,Q,K,S,E)
3	0GM447000 65//	AC	N	C	Extension spring	
4	0GM731336 07//	AC	N	C	Hook (R)/White	(G,W)
	0GM731336 17//	AC	N	C	Hook (R)/Black	(U,Y,H,Q,K,S,E)
5	0GM811000 51//	AD	N	C	Sound proofing tube	
6	0GM911336 23//	AZ	N	C	Ass'y,LCD/EL connection (with shrink tube)	
7	DUNT−2229ACZZ	CE	N	E	LCD display ass'y (35200026)	
8	VHPPW17−256A1	BM	N	D	EL Panel (PW17−256A1)(92133602)	
9	PZETV1042ACZZ	AE	N	C	Insulation sheet 2 (8×15)(81400082)	
12	0GM602015 08//	AD	N	C	Caution label 12×93㎜	
13	XUPSD30P08000	AA		C	Screw (3×8)(41200274)	
14	0GM731336 09//	AD	N	C	Cover A/White	(G,W)
	0GM731336 19//	AD	N	C	Cover A/Black	(U,Y,H,Q,K,S,E)
15	0GM921336 03//	AT	N	C	Roll damper left	
16	0GM921336 04//	AT	N	C	Roll damper right	
17	0GM401336 00//	AC	N	C	Hold angle	
18	XBPSD30P08000	AA		C	Screw (3×8)(41100506)	
19	PZETV1041ACZZ	AE	N	C	Insulation sheet 1 (20×25)(81400081)	
20	0GM731336 04//	AW	N	D	CAB−D/White	(G,W)
	0GM731336 14//	AW	N	D	CAB−D/Black	(U,Y,H,Q,K,S,E)
21	0GM602015 15//	AE	N	C	Decol sheet/White	(G,W)
	0GM602015 16//	AE	N	C	Decol sheet/Black	(U,Y,H,Q,K,S,E)
22	0GM602015 41//	AH	N	C	Pop label	(PC−4641 only)
23	0GM602015 19//	AF	N	C	LED panel,cabinet unit/White	(PC−4641‥G,W)
	0GM602015 20//	AF	N	C	LED panel,cabinet unit/Black	(PC−4641‥U,Y,H,Q,K,S,E)
	0GM602015 17//	AF	N	C	LED panel,cabinet unit/White	(PC−4602‥G,W)
	0GM602015 18//	AF	N	C	LED panel,cabinet unit/Black	(PC−4602‥U,Y,H,Q,K,S,E)
24	0GM812001 02//	AD	N	C	Heat shrinkable tube	
25	VRD−RC2EY102J	AA		C	Resistor (1/4W 1.0KΩ ±5%)(10910252)	
26	GLEGG1024CCZZ	AA		C	Rubber foot (80400060)	
27	0GM602615 40//	AB	N	C	DBP NO label	(G,W)
28	0GM731336 02//	BE	N	D	Cab−B/White	(G,W)
	0GM731336 12//	BE	N	D	Cab−B/Black	(U,Y,H,Q,K,S,E)
29	0GM401336 04//	AD	N	C	Install angle,roll damper	
30	XBPSD30P06000	AA		C	Screw (3×6)(41100504)	
31	0GM921262 19//	AE	N	C	Cable ass'y	
32	0GM701133 60//	AC	N	C	PWB,for LED (without parts)	
33	VHPGL3NG43/−1	AA		B	LED(Green) (GL3NG43)(33499901)	
34	VHPGL3HD43/−1	AB		B	LED(Red) (GL3HD43)(33499902)	
35	QSW−P1067ACZZ	AD		B	Push switch (51700216)	
36	LX−BZ1147CCZZ	AA		C	Screw (41200335)	
37	DUNTK2232ACZZ	CC	N	C	HDD controller with core (92133757)	(PC−4641 only)
38	XBPSD30P04000	AA		C	Screw (3×4)(41100512)	(PC−4641 only)
39	0GM814000 81//	AH	N	C	Fish paper	(PC−4641 only)
40	0GM401335 00//	AL	N	C	Heatsink,power supply	
41	0GM1335//////	BZ	N	E	Power supply unit	
42	PZETV1043ACZZ	AE	N	C	Insulation sheet 4 (25×34)(81400084)	
43	0GM921336 00//	AW	N	C	Power cable	
44	TLABP1317ACSA	AB		C	VR−IND label/Black (60201074−2)	(U,Y,H,Q,K,S,E)
	TLABP1317ACZZ	AB		C	VR−IND label/White (60201074−1)	(G,W)
45	DUNT−2228ACZZ	BK	N	E	Ass'y,keyboard (92133642)	(G)
	DUNT−2226ACZZ	BK	N	E	Ass'y,keyboard (92133641)	(U,Y,Q,S,K,E)
	DUNT−2227ACZZ	BK	N	E	Ass'y,keyboard (92133643)	(H)
	DUNT−2307ACZZ	BK	N	E	Ass'y,keyboard (92133644)	(W)
46	XBPSC30P08000	AA		C	Screw (3×8)(41100510)	(G,W)
	XBPSF30P08000	AA		C	Screw (M3×8)(41100568)	(U,Y,H,Q,K,S,E)
47	GLEGG1019CCZZ	AB		C	Rubber foot (80400039)	
48	0GM731336 01//	BC	N	D	Cab−A/White	(G,W)
	0GM731336 11//	BC	N	D	Cab−A/Black	(U,Y,H,Q,K,S,E)
49	RALMB1007HCZZ	AK		C	Alarm (8Ω)(56100033)	
50	JHNDP1005ACZZ	AF		D	Handle/White (73126235−1)	(G,W)
	JHNDP1005ACSA	AF		D	Handle/Black (73126235−2)	(U,Y,H,Q,K,S,E)
51	0GM401336 10//	AD	N	C	Mesh plate	(G,W)
52	0GM602015 13//	AD	N	C	SIO label	(G,W)
	0GM602015 14//	AD	N	C	SIO label	(U,Y,H,Q,K,S,E)
53	0GM921308 11//	AD	N	C	Speaker OR SW cable	
54	DUNTK2296RHZZ	**	N	E	Main logic PWB ass'y	(PC−4602‥U,Y,S,K,E)
	DUNTK2295RHZZ	**	N	E	Main logic PWB ass'y	(PC−4602‥H,Q)
	DUNTK2333RHZZ	**	N	E	Main logic PWB ass'y	(PC−4602‥G,W)
	DUNTK2294RHZZ	**	N	E	Main logic PWB ass'y	(PC−4641‥U,Y,S,K,E)
	DUNTK2253RHZZ	**	N	E	Main logic PWB ass'y	(PC−4641‥H,Q)
	DUNTK2332RHZZ	**	N	E	Main logic PWB ass'y	(PC−4641‥G,W)
55	0GM401336 05//	AG	N	C	Conn angle,cab unit	
56	LX−BZ1141CCZZ	AA		C	Screw (40133609)	
57	0GM816000 13//	AD	N	C	CONN cover,9P	
58	0GM816000 12//	AD	N	C	CONN cover,25P	
59	XUPSD30P06000	AA		C	Screw (3×6)(41200271)	

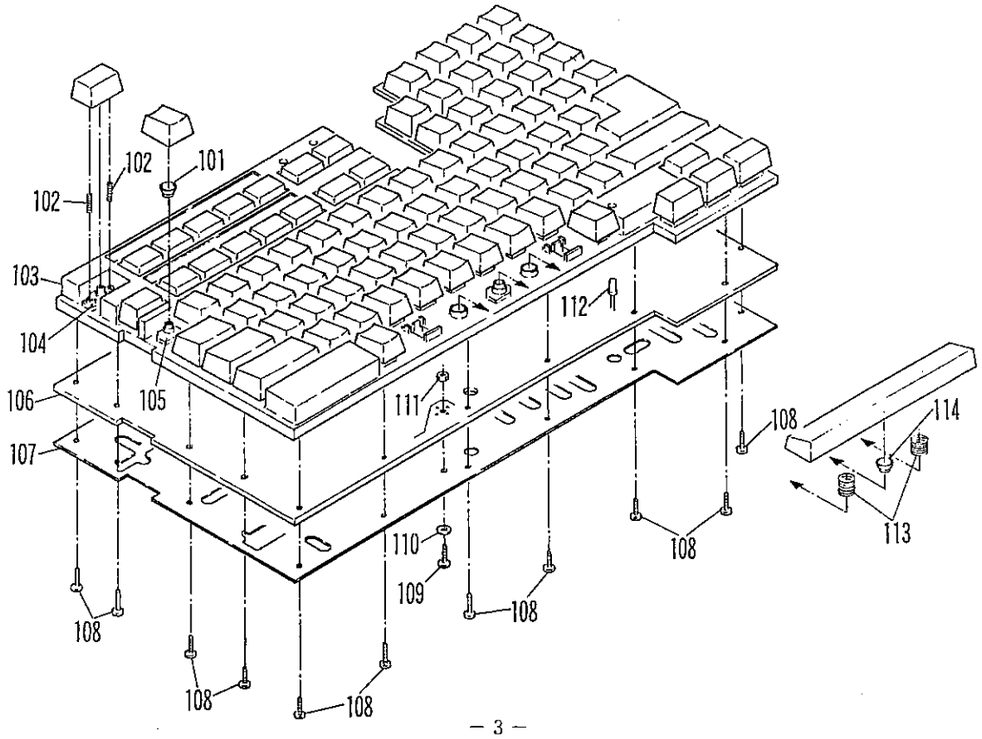
PC4602

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
60	0GM921337 56//	AY	N	C	Single FDD cable	(PC−4641 only)
61	DUNTK2230ACZZ	BU	N	E	FDD(office gray) (92133695)	(G,W)
	DUNTK2230ACSA	BU	N	E	FDD(asphalt gray) (92133605)	(U,Y,H,Q,K,S,E)
62	LX−BZ1182CCZZ	AB		C	Screw (41100517)	
63	PGUMM1562CCZZ	AE		C	Rubber (80400062)	
64	0GM401336 06//	AP	N	C	Ingtall angle	
65	DUNTK2231ACZZ	**	N	D	Hard disk 40MH (92133750)	(PC−4641 only)
66	QCNW−1239ACZZ	AB		C	FDD GD cable (92126226)	
67	0GM813000 95//	AB	N	C	Spacer	(PC−4641 only)
68	0GM543000 20//	BC	N	B	Fan	(PC−4641 only)
69	0GM411006 13//	AD	N	C	Screw (3×23)	(PC−4641 only)
71	UBATZ1003ACZA	BA		A	Battery (83400012)	
72	0GM731336 05//	AN	N	C	Battery cover/White	(G,W)
	0GM731336 15//	AN	N	C	Battery cover/Black	(U,Y,H,Q,K,S,E)
73	LX−BZ1027ACSA	AB		C	Screw (41100570)	(U,Y,H,Q,K,S,E)
	LX−BZ1027ACZZ	AB		C	Screw (41100508)	(G,W)
74	0GM921336 70//	AY	N	C	Double FDD cable	(PC−4602 only)
75	0GM701133 61//	AC	N	C	PWB for S/S switch & AC adaptor jack (without parts)	
76	0GM401336 11//	AC	N	C	Cover plate/White	(G,W)
	0GM401336 12//	AC	N	C	Cover plate/Black	(U,Y,H,Q,S,K,E)

2 Keyboard





2 Keyboard

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0CFR562761/01	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/01	AH	N	C	Half key (H)
	0CFR562763/01	AH	N	C	Half key (G)
	0CFR562830-01	AH	N	C	Half key (W)
2	0CFR562761/02	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/02	AH	N	C	Half key (H)
	0CFR562763/02	AH	N	C	Half key (G)
	0CFR562830-02	AH	N	C	Half key (W)
3	0CFR562761/03	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/03	AH	N	C	Half key (H)
	0CFR562763/03	AH	N	C	Half key (G)
	0CFR562830-03	AH	N	C	Half key (W)
4	0CFR562761/04	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/04	AH	N	C	Half key (H)
	0CFR562763/04	AH	N	C	Half key (G)
	0CFR562830-04	AH	N	C	Half key (W)
5	0CFR562761/05	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/05	AH	N	C	Half key (H)
	0CFR562763/05	AH	N	C	Half key (G)
	0CFR562830-05	AH	N	C	Half key (W)
6	0CFR562761/06	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/06	AH	N	C	Half key (H)
	0CFR562763/06	AH	N	C	Half key (G)
	0CFR562830-06	AH	N	C	Half key (W)
7	0CFR562761/07	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/07	AH	N	C	Half key (H)
	0CFR562763/07	AH	N	C	Half key (G)
	0CFR562830-07	AH	N	C	Half key (W)
8	0CFR562761/08	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/08	AH	N	C	Half key (H)
	0CFR562763/08	AH	N	C	Half key (G)
	0CFR562830-08	AH	N	C	Half key (W)
9	0CFR562761/09	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/09	AH	N	C	Half key (H)
	0CFR562763/09	AH	N	C	Half key (G)
	0CFR562830-09	AH	N	C	Half key (W)
10	0CFR562761/10	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/10	AH	N	C	Half key (H)
	0CFR562763/10	AH	N	C	Half key (G)
	0CFR562830-10	AH	N	C	Half key (W)
11	0CFR562761/11	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/11	AH	N	C	Half key (H)
	0CFR562763/11	AH	N	C	Half key (G)
	0CFR562830-11	AH	N	C	Half key (W)
12	0CFR562761/12	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/12	AH	N	C	Half key (H)
	0CFR562763/12	AH	N	C	Half key (G)
	0CFR562830-12	AH	N	C	Half key (W)
13	0CFR562761/13	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/13	AH	N	C	Half key (H)
	0CFR562763/13	AH	N	C	Half key (G)
	0CFR562830-13	AH	N	C	Half key (W)
14	0CFR562761/14	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/14	AH	N	C	Half key (H)
	0CFR562763/14	AH	N	C	Half key (G)
	0CFR562830-14	AH	N	C	Half key (W)
15	0CFR562761/15	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/15	AH	N	C	Half key (H)
	0CFR562763/15	AH	N	C	Half key (G)
	0CFR562830-15	AH	N	C	Half key (W)
16	0CFR562761/16	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/16	AH	N	C	Half key (H)
	0CFR562763/16	AH	N	C	Half key (G)
	0CFR562830-16	AH	N	C	Half key (W)
17	0CFR562761/17	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/17	AG	N	C	Key top (H)
	0CFR562763/17	AG	N	C	Key top (G)
	0CFR562830-17	AG	N	C	Key top (W)
18	0CFR562761/18	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/18	AG	N	C	Key top (H)
	0CFR562763/18	AG	N	C	Key top (G)
	0CFR562830-18	AG	N	C	Key top (W)
19	0CFR562761/19	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/19	AG	N	C	Key top (H)
	0CFR562763/19	AG	N	C	Key top (G)
	0CFR562830-19	AG	N	C	Key top (W)
20	0CFR562761/20	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/20	AG	N	C	Key top (H)
	0CFR562763/20	AG	N	C	Key top (G)
	0CFR562830-20	AG	N	C	Key top (W)

2 Keyboard

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
21	0CFR562761/21	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/21	AG	N	C	Key top (H)
	0CFR562763/21	AG	N	C	Key top (G)
	0CFR562830-21	AG	N	C	Key top (W)
22	0CFR562761/22	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/22	AG	N	C	Key top (H)
	0CFR562763/22	AG	N	C	Key top (G)
	0CFR562830-22	AG	N	C	Key top (W)
23	0CFR562761/23	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/23	AG	N	C	Key top (H)
	0CFR562763/23	AG	N	C	Key top (G)
	0CFR562830-23	AG	N	C	Key top (W)
24	0CFR562761/24	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/24	AG	N	C	Key top (H)
	0CFR562763/24	AG	N	C	Key top (G)
	0CFR562830-24	AG	N	C	Key top (W)
25	0CFR562761/25	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/25	AG	N	C	Key top (H)
	0CFR562763/25	AG	N	C	Key top (G)
	0CFR562830-25	AG	N	C	Key top (W)
26	0CFR562761/26	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/26	AG	N	C	Key top (H)
	0CFR562763/26	AG	N	C	Key top (G)
	0CFR562830-26	AG	N	C	Key top (W)
27	0CFR562761/27	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/27	AG	N	C	Key top (H)
	0CFR562763/27	AG	N	C	Key top (G)
	0CFR562830-27	AG	N	C	Key top (W)
28	0CFR562761/28	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/28	AG	N	C	Key top (H)
	0CFR562763/28	AG	N	C	Key top (G)
	0CFR562830-28	AG	N	C	Key top (W)
29	0CFR562761/29	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/29	AG	N	C	Key top (H)
	0CFR562763/29	AG	N	C	Key top (G)
	0CFR562830-29	AG	N	C	Key top (W)
30	0CFR562761/30	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/30	AG	N	C	Key top (H)
	0CFR562763/30	AG	N	C	Key top (G)
	0CFR562830-30	AG	N	C	Key top (W)
31	0CFR562761/31	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/31	AG	N	C	Key top (H)
	0CFR562763/31	AG	N	C	Key top (G)
	0CFR562830-31	AG	N	C	Key top (W)
32	0CFR562761/32	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/32	AG	N	C	Key top (H)
	0CFR562763/32	AG	N	C	Key top (G)
	0CFR562830-32	AG	N	C	Key top (W)
33	0CFR562761/33	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/33	AG	N	C	Key top (H)
	0CFR562763/33	AG	N	C	Key top (G)
	0CFR562830-33	AG	N	C	Key top (W)
34	0CFR562761/34	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/34	AG	N	C	Key top (H)
	0CFR562763/34	AG	N	C	Key top (G)
	0CFR562830-34	AG	N	C	Key top (W)
35	0CFR562761/35	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/35	AG	N	C	Key top (H)
	0CFR562763/35	AG	N	C	Key top (G)
	0CFR562830-35	AG	N	C	Key top (W)
36	0CFR562761/36	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/36	AG	N	C	Key top (H)
	0CFR562763/36	AG	N	C	Key top (G)
	0CFR562830-36	AG	N	C	Key top (W)
37	0CFR562761/37	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/37	AG	N	C	Key top (H)
	0CFR562763/37	AG	N	C	Key top (G)
	0CFR562830-37	AG	N	C	Key top (W)
38	0CFR562761/38	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/38	AG	N	C	Key top (H)
	0CFR562763/38	AG	N	C	Key top (G)
	0CFR562830-38	AG	N	C	Key top (W)
39	0CFR562761/39	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/39	AG	N	C	Key top (H)
	0CFR562763/39	AG	N	C	Key top (G)
	0CFR562830-39	AG	N	C	Key top (W)
40	0CFR562761/40	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/40	AG	N	C	Key top (H)
	0CFR562763/40	AG	N	C	Key top (G)
	0CFR562830-40	AG	N	C	Key top (W)

2 Keyboard

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
41	0CFR562761/41	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/41	AG	N	C	Key top (H)
	0CFR562763/41	AG	N	C	Key top (G)
	0CFR562830-41	AG	N	C	Key top (W)
42	0CFR562761/42	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/42	AG	N	C	Key top (H)
	0CFR562763/42	AG	N	C	Key top (G)
	0CFR562830-42	AG	N	C	Key top (W)
43	0CFR562761/43	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/43	AG	N	C	Key top (H)
	0CFR562763/43	AG	N	C	Key top (G)
	0CFR562830-43	AG	N	C	Key top (W)
44	0CFR562761/44	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/44	AG	N	C	Key top (H)
	0CFR562763/44	AG	N	C	Key top (G)
	0CFR562830-44	AG	N	C	Key top (W)
45	0CFR562761/45	AN	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/45	AN	N	C	Key top (H)
	0CFR562763/45	AN	N	C	Key top (G)
	0CFR562830-45	AN	N	C	Key top (W)
46	0CFR562761/46	AH	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/46	AH	N	C	Key top (H)
	0CFR562763/46	AH	N	C	Key top (G)
	0CFR562830-46	AH	N	C	Key top (W)
47	0CFR562761/47	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/47	AG	N	C	Key top (H)
	0CFR562763/47	AG	N	C	Key top (G)
	0CFR562830-47	AG	N	C	Key top (W)
48	0CFR562761/48	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/48	AG	N	C	Key top (H)
	0CFR562763/48	AG	N	C	Key top (G)
	0CFR562830-48	AG	N	C	Key top (W)
49	0CFR562761/49	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/49	AG	N	C	Key top (H)
	0CFR562763/49	AG	N	C	Key top (G)
	0CFR562830-49	AG	N	C	Key top (W)
50	0CFR562761/50	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/50	AG	N	C	Key top (H)
	0CFR562763/50	AG	N	C	Key top (G)
	0CFR562830-50	AG	N	C	Key top (W)
51	0CFR562761/51	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/51	AG	N	C	Key top (H)
	0CFR562763/51	AG	N	C	Key top (G)
	0CFR5.62830-51	AG	N	C	Key top (W)
52	0CFR562761/52	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/52	AG	N	C	Key top (H)
	0CFR562763/52	AG	N	C	Key top (G)
	0CFR562830-52	AG	N	C	Key top (W)
53	0CFR562761/53	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/53	AG	N	C	Key top (H)
	0CFR562763/53	AG	N	C	Key top (G)
	0CFR562830-53	AG	N	C	Key top (W)
54	0CFR562761/54	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/54	AG	N	C	Key top (H)
	0CFR562763/54	AG	N	C	Key top (G)
	0CFR562830-54	AG	N	C	Key top (W)
55	0CFR562761/55	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/55	AG	N	C	Key top (H)
	0CFR562763/55	AG	N	C	Key top (G)
	0CFR562830-55	AG	N	C	Key top (W)
56	0CFR562761/56	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/56	AG	N	C	Key top (H)
	0CFR562763/56	AG	N	C	Key top (G)
	0CFR562830-56	AG	N	C	Key top (W)
57	0CFR562761/57	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/57	AG	N	C	Key top (H)
	0CFR562763/57	AG	N	C	Key top (G)
	0CFR562830-57	AG	N	C	Key top (W)
58	0CFR562761/58	AH	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/58	AH	N	C	Key top (H)
	0CFR562763/58	AH	N	C	Key top (G)
	0CFR562830-58	AH	N	C	Key top (W)
59	0CFR562761/59	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/59	AG	N	C	Key top (H)
	0CFR562763/59	AG	N	C	Key top (G)
	0CFR562830-59	AG	N	C	Key top (W)
60	0CFR562761/60	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/60	AG	N	C	Key top (H)
	0CFR562763/60	AG	N	C	Key top (G)
	0CFR562830-60	AG	N	C	Key top (W)

2 Keyboard

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
61	0CFR562761/61	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/61	AG	N	C	Key top (H)
	0CFR562763/61	AG	N	C	Key top (G)
	0CFR562830-61	AG	N	C	Key top (W)
62	0CFR562761/62	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/62	AG	N	C	Key top (H)
	0CFR562763/62	AG	N	C	Key top (G)
	0CFR562830-62	AG	N	C	Key top (W)
63	0CFR562761/63	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/63	AG	N	C	Key top (H)
	0CFR562763/63	AG	N	C	Key top (G)
	0CFR562830-63	AG	N	C	Key top (W)
64	0CFR562761/64	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/64	AG	N	C	Key top (H)
	0CFR562763/64	AG	N	C	Key top (G)
	0CFR562830-64	AG	N	C	Key top (W)
65	0CFR562761/65	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/65	AG	N	C	Key top (H)
	0CFR562763/65	AG	N	C	Key top (G)
	0CFR562830-65	AG	N	C	Key top (W)
66	0CFR562761/66	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/66	AG	N	C	Key top (H)
	0CFR562763/66	AG	N	C	Key top (G)
	0CFR562830-66	AG	N	C	Key top (W)
67	0CFR562761/67	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/67	AG	N	C	Key top (H)
	0CFR562763/67	AG	N	C	Key top (G)
	0CFR562830-67	AG	N	C	Key top (W)
68	0CFR562761/68	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/68	AG	N	C	Key top (H)
	0CFR562763/68	AG	N	C	Key top (G)
	0CFR562830-68	AG	N	C	Key top (W)
69	0CFR562761/69	AK	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/69	AK	N	C	Key top (H)
	0CFR562763/69	AK	N	C	Key top (G)
	0CFR562830-69	AK	N	C	Key top (W)
70	0CFR562761/70	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/70	AG	N	C	Key top (H)
	0CFR562763/70	AG	N	C	Key top (G)
	0CFR562830-70	AG	N	C	Key top (W)
71	0CFR562761/71	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/71	AG	N	C	Key top (H)
	0CFR562763/71	AG	N	C	Key top (G)
	0CFR562830-71	AG	N	C	Key top (W)
72	0CFR562761/72	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/72	AG	N	C	Key top (H)
	0CFR562763/72	AG	N	C	Key top (G)
	0CFR562830-72	AG	N	C	Key top (W)
73	0CFR562761/73	AM	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/73	AM	N	C	Key top (H)
	0CFR562763/73	AM	N	C	Key top (G)
	0CFR562830-73	AM	N	C	Key top (W)
74	0CFR562761/74	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/74	AG	N	C	Key top (H)
	0CFR562763/74	AG	N	C	Key top (G)
	0CFR562830-74	AG	N	C	Key top (W)
75	0CFR562761/75	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/75	AH	N	C	Half key (H)
	0CFR562763/75	AH	N	C	Half key (G)
	0CFR562830-75	AH	N	C	Half key (W)
76	0CFR562761/76	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/76	AH	N	C	Half key (H)
	0CFR562763/76	AH	N	C	Half key (G)
	0CFR562830-76	AH	N	C	Half key (W)
77	0CFR562761/77	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/77	AH	N	C	Half key (H)
	0CFR562763/77	AH	N	C	Half key (G)
	0CFR562830-77	AH	N	C	Half key (W)
78	0CFR562761/78	AH	N	C	Half key (U,Y,Q,S,K,E)
	0CFR562762/78	AH	N	C	Half key (H)
	0CFR562763/78	AH	N	C	Half key (G)
	0CFR562830-78	AH	N	C	Half key (W)
79	0CFR562761/79	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/79	AG	N	C	Key top (H)
	0CFR562763/79	AG	N	C	Key top (G)
	0CFR562830-79	AG	N	C	Key top (W)
80	0CFR562761/80	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/80	AG	N	C	Key top (H)
	0CFR562763/80	AG	N	C	Key top (G)
	0CFR562830-80	AG	N	C	Key top (W)

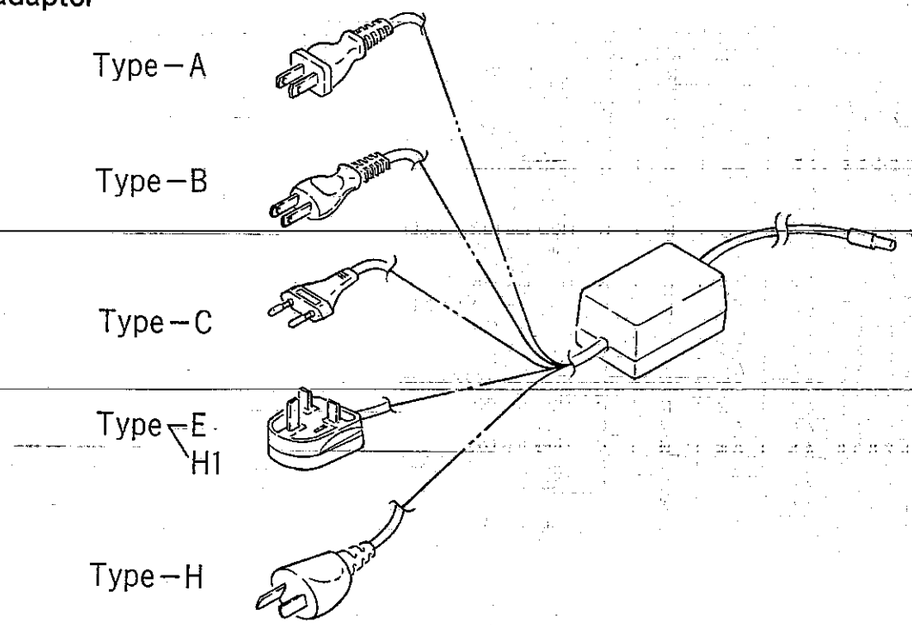
2 Keyboard

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
81	0CFR562761/81	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/81	AG	N	C	Key top (H)
	0CFR562763/81	AG	N	C	Key top (G)
	0CFR562830-81	AG	N	C	Key top (W)
82	0CFR562761/82	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/82	AG	N	C	Key top (H)
	0CFR562763/82	AG	N	C	Key top (G)
	0CFR562830-82	AG	N	C	Key top (W)
83	0CFR562761/83	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/83	AG	N	C	Key top (H)
	0CFR562763/83	AG	N	C	Key top (G)
	0CFR562830-83	AG	N	C	Key top (W)
84	0CFR562761/84	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/84	AG	N	C	Key top (H)
	0CFR562763/84	AG	N	C	Key top (G)
	0CFR562830-84	AG	N	C	Key top (W)
85	0CFR562761/85	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/85	AG	N	C	Key top (H)
	0CFR562763/85	AG	N	C	Key top (G)
	0CFR562830-85	AG	N	C	Key top (W)
86	0CFR562761/86	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/86	AG	N	C	Key top (H)
	0CFR562763/86	AG	N	C	Key top (G)
	0CFR562830-86	AG	N	C	Key top (W)
87	0CFR562761/87	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/87	AG	N	C	Key top (H)
	0CFR562763/87	AG	N	C	Key top (G)
	0CFR562830-87	AG	N	C	Key top (W)
88	0CFR562761/88	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/88	AG	N	C	Key top (H)
	0CFR562763/88	AG	N	C	Key top (G)
	0CFR562830-88	AG	N	C	Key top (W)
89	0CFR562761/89	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/89	AG	N	C	Key top (H)
	0CFR562763/89	AG	N	C	Key top (G)
	0CFR562830-89	AG	N	C	Key top (W)
90	0CFR562761/90	AG	N	C	Key top (U,Y,Q,S,K,E)
	0CFR562762/90	AG	N	C	Key top (H)
	0CFR562763/90	AG	N	C	Key top (G)
	0CFR562830-90	AG	N	C	Key top (W)
101	0CF567664C///	AA	N	C	Rubber RT
102	0CF56A185F///	AA		C	Spring for half key
103	0CF56B036A///	AQ	N	C	Frame (G,W)
	0CF56B036B///	AQ	N	C	Frame (U,Y,Q,S,K,E,H)
104	0CF565665A///	AB		C	Switch for half key
105	0CF565524B///	AB	N	C	Switch
106	0CF56H089B///	BD	N	C	PWB (G,H,W)
	0CF56H089A///	BD	N	C	PWB (U,Y,Q,S,K,E)
107	0CF56A514B///	AK	N	C	Shield plate
108	0CF564965C///	AA		C	Screw (M2×6)
109	0CF560088B///	AA		C	Screw (M3×5)
110	0CF561565A///	AA		C	Washer (M3)
111	0CF560940A///	AA		C	Nut (M3×0.5)
112	0CF565033M///	AD	N	B	LED-R
113	0CF567955A///	AA	N	C	Spring C for space key
114	0CF567664D///	AA	N	C	Rubber RT for space key
	(Unit)				
901	DUNT-2228ACZZ	BK	N	E	Ass'y,keyboard (92133642) (G)
	DUNT-2226ACZZ	BK	N	E	Ass'y,keyboard (92133641) (U,Y,Q,S,K,E)
	DUNT-2227ACZZ	BK	N	E	Ass'y,keyboard (92133643) (H)
	DUNT-2307ACZZ	BK	N	E	Ass'y,keyboard (92133644) (W)

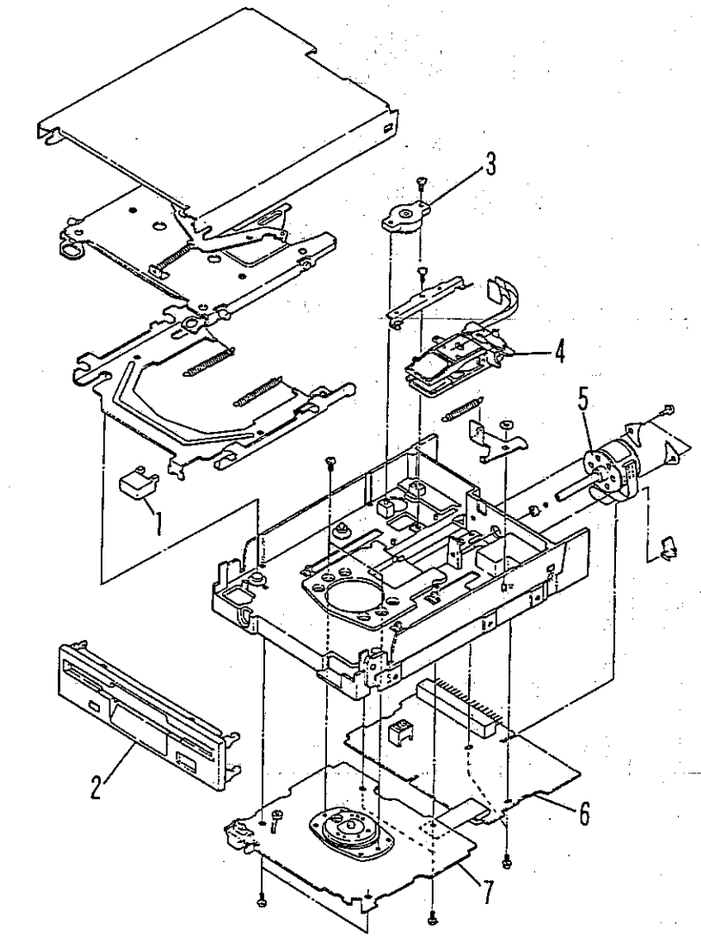
3 AC adaptor

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RADPA1004ACZZ	BP		B	AC adaptor(92126220)(120V) (Type-A)
	RADPA1011ACZZ	BQ		B	AC adaptor(92130755)(120V) (Type-A) (U)
	RADPA1008ACZA	BP		B	AC adaptor(92128420)(220V) (Type-C) (Y)
	RADPA1007ACZZ	BP		B	AC adaptor(92133654)(240V) (Type-E) (G,K,W)
	CADPA1005AC01	BQ		B	AC adaptor(92133656)(240V) (Type-H1) (H)
	RADPA1006ACZZ	BQ		B	AC adaptor(92130754)(240V) (Type-H) (S)
	RADPA1013ACZZ	BQ	N	B	AC adaptor(option)(100V)(Type-A) (Q)
	RADPA1004ACZZ	BP		B	AC adaptor(option)(120V)(Type-A) (EJ)
	RADPA1010ACZZ	BP		B	AC adaptor(option)(110V)(Type-A) (ESC)
	RADPA1006ACZZ	BQ		B	AC adaptor(option)(240V)(Type-H) (ESC1)
	RADPA1007ACZZ	BP		B	AC adaptor(option)(240V)(Type-E) (EQ)
	RADPA1008ACZA	BP		B	AC adaptor(option)(220V)(Type-C) (EH)
	RADPA1009ACZZ	BP		B	AC adaptor(option)(220V)(Type-A) (ESG)
	RADPA1012ACZZ	BQ		B	AC adaptor(option)(127V)(Type-A) (ESG1) (ESB)

3 AC adaptor



4 FDD ass'y



4 FDD ass'y

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	00G167880390 9	AC	N	D	Button(office gray) (For DUNTK2230ACZZ)
	00G167880391 0	AC	N	D	Button(asphalt gray) (For DUNTK2230ACSA)
2	00G179676960 9	AH	N	D	Front bezel ass'y(office gray) (For DUNTK2230ACZZ)
	00G179676961 0	AH	N	D	Front bezel ass'y(asphalt gray) (For DUNTK2230ACSA)
3	00G179676769 3//	AH	N	E	Damper ass'y
4	00G179677290 0	BP	N	E	Head carriaage ass'y(Note 1)
5	00G147694300 0	AY	N	E	Stepping motor ass'y
6	00G155321100 5	BL	N	E	PCBA MFD control T
7	00G147340343 2	BM	N	E	Spindle motor ass'y
101	00G149005160 3	CP	N	D	Alignment disk
102	00G149005170 1	CE	N	D	Level disk
	(Unit)				(G,W)
901	DUNTK2230ACZZ	BU	N	E	FDD(office gray) (U,Y,H,Q,K,S,E)
	DUNTK2230ACSA	BU	N	E	FDD(asphalt gray)

5 Power supply ass'y

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VRD-HT2EY122J	AA		C	Resistor (1/4W 1.2KΩ ±5%)(10112251) [R54]
2	VRD-HT2EY2R2J	AA	N	C	Resistor (1/4W 2.2Ω ±5%)(10122851) [R11,26,27]
3	VRD-HT2EY101J	AA		C	Resistor (1/2W 100Ω ±5%)(10210151) [R25]
4	VRD-HT2HY221J	AB		C	Resistor (1/2W 220Ω ±5%)(10222151) [R23]
5	VRD-HT2EY102J	AA		C	Resistor (1/4W 1KΩ ±5%)(10510251) [R44,51,53,61]
6	VRD-HT2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%) (10510351) [R3,6,7,12,29,31,45,52,59,64]
7	VRD-HT2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)(10510451) [R1,4,5]
8	VRD-HT2EY120J	AA		C	Resistor (1/4W 12Ω ±5%)(10512051) [R41]
9	VRD-HT2EY163J	AA		C	Resistor (1/4W 16KΩ ±5%) (10516351) [R19,32,49,56,63]
10	VRD-HT2EY222J	AA		C	Resistor (1/4W 2.2KΩ ±5%) (10522251) [R14,17,20,36,50]
11	VRD-HT2EY224J	AA		C	Resistor (1/4W 220KΩ ±5%)(10522451) [R2]
12	VRD-HT2EY271J	AA		C	Resistor (1/4W 270Ω ±5%)(10527151) [R35]
13	VRD-HT2EY332J	AA		C	Resistor (1/4W 3.3KΩ ±5%) (10533251) [R21,28,30,34,37]
14	VRD-HT2EY272J	AA	N	C	Resistor (1/4W 2.7KΩ ±5%) [R18]
15	VRD-HT2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%) (10547251) [R9,10,13,22,24,58]
16	VRD-HT2EY561J	AA		C	Resistor (1/4W 560Ω ±5%)(10556151) [R8]
17	VRD-HT2EY562J	AA		C	Resistor (1/4W 5.6KΩ ±5%)(10556251) [R40]
18	VRD-HT2EY822J	AA		C	Resistor (1/4W 8.2KΩ ±5%)(10582251) [R33]
19	VRNHT2EK1072F	AA	N	C	Resistor (1/4W 10.7KΩ ±1%)(11010721) [R43]
20	VRNHT2EK1241F	AA	N	C	Resistor (1/4W 1.24KΩ ±1%)(11012411) [R46]
21	VRNHT2EK4122F	AA	N	C	Resistor (1/4W 41.2KΩ ±1%)(11041221) [R57]
22	0GM1336295 0//	AD	N	C	Resistor (3W 0.62R 5%) [R15]
23	0GM1812022 0//	AF	N	C	Variable resistor (2KΩ) [VR2]
24	RVR-P1009ACZZ	AE	N	B	Variable resistor (20KΩ)(18120390) [VR3,4]
25	0GM1813030 1//	AF	N	C	Variable resistor (30KΩ) [VR6]
26	0GM1815020 2//	AF	N	B	Variable resistor (5KΩ) [VR1]
27	0GM2021035 9//	AB	N	C	Capacitor (0.01μF) [C20]
28	0GM2024730 2//	AB	N	C	Capacitor (0.047μF) [C8,10,11,12]
29	0GM2025610 5//	AB	N	C	Capacitor (560pF 500V) [C36]
30	RC-KZ105 4CCZZ	AB		C	Capacitor (0.1μF 50V)(20310400) [C1~4,38]
31	VCQYNU1HM473K	AB		C	Capacitor (0.047μF)(22147302) [C16,19]
32	0GM2412280 0//	AG	N	C	Capacitor (2200μF 16V) [C5,40]
33	VCEAEU1HW105M	AA	N	C	Capacitor (1μF 50V)(24210525) [C33]
34	0GM2421061 8//	AC	N	C	Capacitor (10μF 16V) [C9,23]
35	0GM2421063 1//	AC	N	C	Capacitor (10μF 6.3V) [C18]
36	0GM2421082 7//	AD	N	C	Capacitor (1000μF 6.3V) [C13,14]
37	VHi79M12AUC-1	AP	N	B	IC (79L12) [C24]
38	0GM2422261 9//	AC	N	C	Capacitor (22μF 50V) [C17,32]
39	0GM2422270 2//	AB	N	C	Capacitor (220μF 16V) [C15,21,27]
40	0GM2423360 3//	AB	N	C	Capacitor (33μF 16V) [C25,26]
41	0GM2423361 1//	AC	N	C	Capacitor (33μF 35V) [C41]
42	0GM2423361 2//	AC	N	C	Capacitor (33μF 25V) [C7]
43	0GM2424750 1//	AB	N	C	Capacitor (4.7μF 25V) [C6]
44	0GM2424771 5//	AB	N	C	Capacitor (470μF 10V) [U2,3,7]
45	0GM3110431 0//	AF	N	B	Shunt regulator (UA431) [U5]
46	0GM3111070 0//	BB	N	B	SA switching(LT1071) [U1]
47	VHiMN1280T/-1	AE		B	IC regulator (MN1280T)(31112800) [U6]
48	0GM3117905 2//	AF	N	B	IC (79L05) [Q18]
49	0GM3210200 0//	AG	N	B	Transistor (NPN MJE200) [Q2~4,8~11,14,15,19,20,21,25,26,38]
50	0GM3211213 1//	AC	N	B	Transistor (2SC1213A NPN) [Q17,35]
51	0GM3218050 0//	AB	N	B	Transistor (8050 NPN) [Q22]
52	0GM3220450 5//	AL	N	B	Transistor (D45H5 TO-220) [Q1,5,6,7,16,23,39]
53	VS2SA673AB/-1	AE		B	Transistor (2SA673A)(32206730) [Q40]
54	0GM3221443 0//	AP	N	B	Transistor (PNP 2SA1443) [Q12,13]
55	0GM3221444 0//	AQ	N	B	Transistor (PNP 2SA1444) [Q24,29,31]
56	0GM3228550 0//	AB	N	B	Transistor (LM8550 PNP) [D11,13,17,20,21]
57	0GM3310100 4//	AB	N	B	Diode (1F1 1A) [D1]
58	0GM3310104 0//	AR	N	B	Dual diode (S10SC4M)

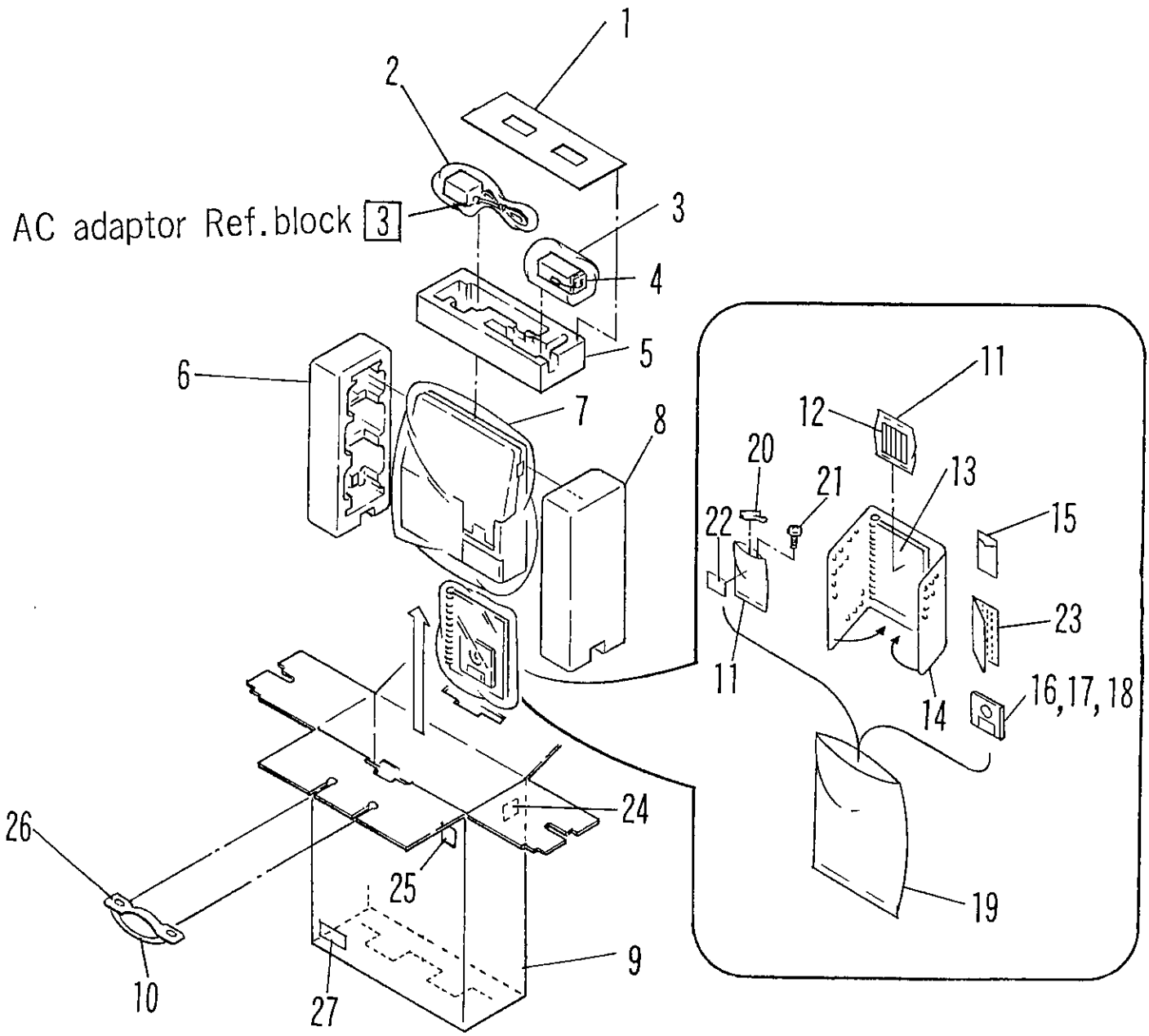
5 Power supply ass'y

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
59	0GM33103035//	AH	N	B	Schottky diode (SR303) [D16]
60	0GM33105301//	AQ	N	B	Schottky diode (5A 30V) [D6,25]
61	VHD1N4148//−1	AA		B	Diode (1N4148)(33241480) [D3~5,7,8,9,12,23,24,30]
62	VHEHZ3ALL//−1	AC		B	Zener diode (HZ3ALL)(33300030)
63	0GM33352290//	AB	N	B	Diode (IN5229B)
64	VHD1SS108//−1	AB		B	Diode (1SS108) [ZD2]
65	0GM33352501//	AB	N	B	Zener diode (IN5250B) [D22]
66	0GM40133500//	AL	N	C	Heatsink,power supply [ZD5]
67	XBPSD30P06000	AA		C	Screw (3×6)(41100504)
68	0GM42200085//	AA	N	C	Flat−W-GS ZNH4
69	QCNCM5016SC0B	AA		C	Connector (Fan) (2pin)(50400244)
70	0GM50400364//	AC	N	C	Connector (3pin) [J3]
71	0GM50402627//	AN	N	C	Connector header SO pin [J2]
72	0GM50700007//	AD	N	C	Adaptor jack 2mm SMK (S−G9312) [J1]
73	0GM51400006//	AM	N	C	SW mini slide C&K : L111 series
74	0GM52100030//	AC	N	C	Inductor (100μH)
75	0GM52100171//	AF	N	C	Choke (28μH L−5020) [L1,4]
76	0GM52113351//	AH	N	C	Common mode choke [L5]
77	0GM52113352//	AM	N	C	Common mode choke [T1]
78	0GM52313353//	AQ	N	B	+5V power transformer [T2]
79	0GM52313354//	AP	N	B	+12V power transformer [T3]
80	0GM52313355//	AG	N	B	Power transformer [T4]
81	0GM52313356//	AT	N	B	Power transformer [T5]
82	0GM53113350//	AD	N	A	Fuse (7A 125V) [T6]
83	0GM57113350//	AA	N	C	Wire (190mm)(Orange) [F1]
84	0GM57113351//	AA	N	C	Wire (190mm)(White)
85	0GM70113361//	AC	N	B	PWB,for S/S switch & AC adaptor jack (without parts)
86	PCOVP6633RCZZ	AB		C	Fuse cap(TUV reguration) for F1 (73133630)
87	0GM81000002//	AB	N	C	Insulator TO−220
88	0GM81300012//	AC	N	C	Nylon insulator
89	PZETV1043ACZZ	AE	N	C	Insulation sheet 4 (25×34)(81400084)
90	0GM92133502//	AG	N	C	Battery cable
91	0GM92133510//	AC	N	C	Switch wire ass'y
92	0GM92133600//	AW	N	C	Power cable
93	0GM99100//////	AA	N	C	Heatsink compound #340
94	VCEAEU1AW336M	AA	N	C	Capacitor (33μF 10V)
95	VCEAGU1EW476M	AB		C	Capacitor (47μF 25V) [C30]
96	VCSAVU1CE476M	AH	N	C	Capacitor (47μF 16V) [C31]
	(Unit)				[C39]
901	0GM1335//////	BZ	N	E	Power supply unit

6 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0GM61400728//	AC	N	D	Packing add
2	SSAKH5002CCZZ	AA		D	Vinyl bag (160×380mm)(61200873)
3	SSAKA0019SCZZ	AA		D	Vinyl bag (120×180mm)(61200866)
4	UBATZ1003ACZA	BA		A	Battery (83400012)
5	0GM61336003//	AK	N	D	EPS,accessory (Polyform add)
6	0GM61336002//	AK	N	D	EPS END,Right (Polyform add)
7	SSAKA0006WCZZ	AB		D	Vinyl bag (400×500mm)(61200865)
8	0GM61336001//	AK	N	D	EPS END,Left (Polyform add)
9	0GM61501020//	AS	N	D	Packing case series (PC−4641··U,Y)
	0GM61501019//	AN	N	D	Packing case series (PC−4641··H,Q,G,K,S,E,W)
	0GM61501017//	AS	N	D	Packing case series (PC−4602··U,Y)
	0GM61501016//	AN	N	D	Packing case series (PC−4602··H,Q,G,K,S,E,W)
10	JHNDP5003SCZZ	AB		C	Carrying handle (73126260)
11	SSAKH0011HCZZ	AA		D	Vinyl bag (60×140mm)(61200872)
12	LPLTP1017ACZZ	AB		C	Ten plate (60200960)
13	0GM60300123//	BA	N	D	Operation manual(ENG 3) (H,Q,S,K,E)
	0GM60300121//	AX	N	D	Operation manual(ENG 1) (U)
	0GM60300122//	BG	N	D	Operation manual(ENG 2) (Y)
14	SPAKA1982ACZZ	AE		D	Packing cushion for inst.book (61200874) (U,Y,H,Q,S,K,E)
15	PCASZ2005HCZA	AC		D	Reply post envelope (60100235) (U)
16	0GM60201530//	AC	N	C	Floppy disk label
17	GCASP5017SCZZ	AE	N	D	Floppy disk case (73126255)
18	DFLP−1134ACZZ	BF	N	D	Diskette 3−1/2" (85100004)
19	SSAKH0015HCZZ	AA		D	Vinly bag (180×280mm)(61200867)
20	0GM40133607//	AF	N	C	Modem conn angle(for CE−451M·462M)
21	0GM41100611//	AA	N	C	Screw(for CE−451M·462M) (M3×6)
22	0GM60201524//	AB	N	C	Explanation label
23	0GM60300124//	AG	N	C	Warranty sheet
24	0GM60201509//	AD	N	C	UPC label(Bar code) (Q only)
	0GM60201510//	AB	N	C	UPC label(Bar code) (PC−4602··Y only)
25	TLABM1338ACZZ	AB	N	C	Destination label (60201094) (PC−4641··Y only)
26	SPAKA5416SCZZ	AB		D	Handle packing cushion (61400675) (W)
27	0GM60201522//	AC	N	C	Address label
101	0GM61501018//	AK	N	D	Master packing carton (Y only)
	0GM61501015//	AK	N	D	Master packing carton (PC−4641 only)
					(PC−4602 only)

6 Packing material & Accessories



7 Key top kit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	DUNT-2238ACZZ	—	N	E	CE-460KE Key top kit(English)service parts is not available. only available as sales item
	DUNT-2239ACZZ	—	N	E	CE-460KF Key top kit(France)service parts is not available. only available as sales item
	DUNT-2240ACZZ	—	N	E	CE-460KW Key top kit(Italy,Switzerland)service parts is not available. only available as sales item
	DUNT-2241ACZZ	—	N	E	CE-460KS Key top kit(Scandinavia)service parts is not available. only available as sales item
	DUNT-2242ACZZ	—	N	E	CE-460KM Key top kit(Spain)service parts is not available. only available as sales item

8 Main logic PWB ass'y

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	VRS-TP2BD100J	AA		C	Resistor (1/8W 10Ω ±5%)(10010052)	[R22,28]
2	VRS-TP2BD102J	AA		C	Resistor(1/8W 1.0KΩ ±5%)(10010252)	[R2~7,16,26,37,38]
3	VRS-TP2BD103J	AA		C	Resistor (1/8W 10KΩ ±5%)(10010352)	[R40]
4	VRS-TP2BD104F	AA	N	C	Resistor(1/8W 100KΩ ±1%)(10010412)	[R9,10]
6	VRS-TP2BD104J	AA		C	Resistor (1/8W 100KΩ ±5%)(10010452)	[R14,31,41]
7	VRS-TP2BD105J	AA		C	Resistor(1/8W 1MΩ ±5%)(10010552)	[R21,24,27,34,48]
8	VRS-TP2BD152J	AA		C	Resistor (1/8W 1.5KΩ ±5%)(10015252)	[R42,43,47]
9	VRS-TP2BD153J	AA		C	Resistor (1/8W 15KΩ ±5%)(10015352)	[R33]
10	VRS-TP2BD222J	AA		C	Resistor (1/8W 2.2KΩ ±5%)(10022252)	[R17,19]
11	VRS-TP2BD303F	AA	N	C	Resistor (1/8W 30KΩ ±1%)(10030312)	[R11]
12	VRS-TP2BD333F	AA	N	C	Resistor (1/8W 33KΩ ±1%)(10033312)	[R12]
13	VRS-TP2BD333J	AA		C	Resistor (1/8W 33KΩ ±5%)(10033352)	[R13]
14	VRS-TP2BD392J	AA		C	Resistor (1/8W 3.9KΩ ±5%)(10039252)	[R39]
15	VRS-TP2BD470J	AA		C	Resistor (1/8W 47Ω ±5%)(10047052)	[R18,20,35,46]
16	VRS-TP2BD471J	AA		C	Resistor (1/8W 470Ω ±5%)(10047152)	[R23]
17	VRS-TP2BD474J	AA		C	Resistor (1/8W 470KΩ ±5%)(10047452)	[R8]
18	VRS-TP2BD560J	AA		C	Resistor (1/8W 56Ω ±5%)(10056052)	[R1]
19	VRS-TP2BD562J	AA		C	Resistor (1/8W 5.6KΩ ±5%)(10056252)	[R25]
20	VRS-TP2BD563J	AA		C	Resistor(1/8W 56KΩ ±5%)(10056352)	[R29,30,36,44,45]
	VRS-TP2BD563J	AA		C	Resistor(1/8W 56KΩ ±5%)(10056352)(PC-4641 only)	[R15]
21	VRS-TP2BD683J	AB		C	Resistor (1/8W 68KΩ ±5%)(10068352)	[R32]
22	VRD-RC2EY000J	AA		C	Resistor (1/4W 0Ω ±5%)(10900052)	[J1]
	VRD-RC2EY000J	AA		C	Resistor(1/4W 0Ω ±5%)(10900052)(PC-4602 only)	[J2]
	VRD-RC2EY000J	AA		C	Resistor(1/4W 0Ω ±5%)(10900052)(PC-4641 only)	[J5]
23	RMPTC4102QCJB	AB		B	Resistor array (1KΩ×4 1/8W ±5%)(14010253)	[RN1,3]
24	RMPTC7123QCJB	AC	N	B	Resistor array (12KΩ×7 1/8W ±5%)(14012353)	[RN2]
25	RMPTC4152QCJB	AC	N	B	Resistor farray (1.5KΩ×4 1/8W ±5%)(14015200)	[RN6]
26	RMPTC8472QCJB	AB	N	B	Resistor ntwek (4.7KΩ×8 1/8W ±5%)(14047257)	[RN10]
27	RMPTC4472QCJB	AB		B	Resistor net (4.7KΩ×4 1/8W ±5%)(14047265)	[RN12]
28	RMPTC8563QCJB	AC		B	Resistor array bus (S) (56KΩ×8 1/8W ±5%)(14056251)	[RN8]
29	RMPTC4563QCJB	AB		B	Resistor array (56KΩ×4 1/8W ±5%)(14056350)	[RN7]
30	0GM1414705 1//	AM	N	B	Resistor array (47R 2×8 SMD)	[RN4,5,9,11]
31	VCCCTS1HH100J	AA	N	C	Capacitor (10pF 50V)(20210021)	[C23,27]
32	VCKYTS1HB102K	AA	N	C	Capacitor (1000pF 50V)(20210224)	[C38]
33	VCKYTS1HB103K	AA	N	C	Capacitor (0.01μF 50V)(20210384)	[C41]
34	0GM2021048 6//	AC	N	C	Capacitor(0.1μF)	[C5,7,10,11,16,17,21,29,33,34,35,37,44]
	0GM2021048 6//	AC	N	C	Capacitor (0.1μF)(PC-4641 only)	[C13]
35	VCCCTS1HH150J	AA	N	C	Capacitor(15pF 50V)(20215007)	[C19,20,30,31,39,42]
36	VCCCTS1HH180J	AA	N	C	Capacitor (18pF 50V)(20218003)	[C28]
37	VCCCTS1HH220J	AA	N	C	Capacitor (22pF 50V)(20222009)	[C24,50]
38	VCCCTS1HH330J	AA	N	C	Capacitor (33pF 50V)(20233009)	[C26,32]
	VCCCTS1HH330J	AA	N	C	Capacitor (33pF 50V)(20233009)(U,Y,S,K,E)	[CBS2]
39	VCCCTS1HH470J	AA		C	Capacitor (47pF 50V)(20247012)	[C18,40,46,49,CLCD0~7]
	VCCCTS1HH470J	AA		C	Capacitor (47pF 50V)(20247012)(U,Y,S,K,E)	[CS2]
40	RC-KZ1054CCZZ	AB		C	Capacitor(MN 50V 0.1μF)(20310400)	[C1~4,22,25,43,47]
41	VCEAEU1HW105M	AA	N	C	Capacitor (1μF 50V)(24210525)	[C36]
42	VCEAEA1CW106M	AC	N	C	Capacitor(10μF 16V)(24210609)	[C6,8,9,12,14,15,45,48]
43	0GM3027438 3//	AE	N	B	IC (74LS38)	[U33,36]
44	VHiTC4S71F/-1	AC		B	IC (TC4S71F)(30640713)	[U26]
45	VHiTC4S81F/-1	AC		B	IC (TC4S81F)(30640810)	[U23]
46	VHiM4464-12PZ	AU	N	B	IC(M4464-12PZ)(30704642)	[U1~15,17~21,41~44]
47	VHiLU57844P-1	AU	N	B	IC (LU57844P)(30857840)	[U24]
48	0GM3087020 1//	BU	N	B	IC (UPD70208-10)	[U34]
49	0GM3088250 3//	BK	N	B	IC (82C50A)	[U46]
50	VHiLZ95H12/-1	BA	N	B	IC (LZ95H12)(30913360)	[U29]
51	VHiLZ93J21/-1	BC	N	B	IC (LZ93J21)(30913361)	[U45]
52	VHiTC8566F/-1	BB		B	IC (TC8566F)(30927940)	[U35]
53	0GM3151488 6//	AQ	N	B	IC (14C88)	[U40]
54	0GM3151489 4//	AQ	N	B	IC (14C89A)	[U39]
55	VHiBA6251AF-1	AE	N	B	TR.Array (BA6251F)(31862510)	[U16,47,48]
56	0GM3190431 1//	AF	N	B	IC (TL431C)	[U25]
57	VS2SC2021-/-1	AB		B	Transistor (2SC2021)(32120210)	[Q3]
58	0GM3212712 0//	AB	N	B	XTOR SMD IC (100MA HFE=10D C2712Y)	[Q1,2]
59	VHD1SS108//-1	AB		B	Diode (1SS108)(33001080)	[D4~9]
60	VHDDSS133HV-1	AA		B	Diode (1SS133)(33001330)	[D1~3]
61	VHi27C51AAA0A	BF	N	B	IC EP ROM (27C51AAA0A)(U,Y,S,K,E)	[U22]
	VHi27C51AAA1A	BF	N	B	IC EPROM (27C51AAA1A)(G,H,Q,W)	[U22]

8 Main logic PWB ass'y

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
62	0GM3764125 3//	AG	N	B	IC (74HC125) [U27]
63	0GM3764157 3//	AG	N	B	IC (74HC157) [U32]
64	0GM3767400 3//	AF	N	B	IC (74HC00) [U31]
65	0GM3767404 3//	AE	N	B	IC (74HC04) [U30,37]
66	0GM3767432 3//	AF	N	B	IC (74HC32) [U38]
67	0GM5010250 0//	AK	N	C	CONN Edge 1×25 header [CN6(KEYB)]
68	QSŌCZ6428ACZZ	AE		C	IC socket 28P (50202802) [U22]
69	QSŌCZ6440ACZZ	AG		C	IC socket 40pin LOW profile (50204005) [U28]
70	0GM5030091 7//	AK	N	C	Connector (DB9M) [CN12(SIO)]
71	0GM5030251 8//	AN	N	C	Connector (25pin) [CN9(EXT FDL)CN10(PRINTER)]
72	QCNCM5016SC0B	AA		C	Connector header(2pin) (50400244) [CN2(SW)SN3(SPKR)]
73	QCNCM5016SC0F	AB		C	Connector 1×6 ST Header (6pin)(50400664) [CN4(LED)]
74	QCNCM2303SC0H	AB		C	Connector 1xB ST HDR(8pin)(50400834)(PC−4641 only) [CN15(HDD PWR)]
75	0GM5040141 4//	AD	N	C	Connector header STR 14pin [CN1(LCD)]
76	0GM5040262 5//	AE	N	C	Connector header STR 26pin [CN5(PSU)]
77	0GM5040343 3//	AM	N	C	Connector 2×17 header pan type [CN17(EMS)]
78	0GM5040343 4//	AQ	N	C	Connector headerRT 2×17 shounded [CN13(MODEM)]
79	0GM5040343 5//	AF	N	C	Connector 2×17 header [CN8(FDD)]
80	QCNCM2346SC4J	AL		C	Connector HDR 2x20(40pin)(50404022)(PC−4641 only) [CN14(HDD)]
81	QCNCM00NSSC50	AM		C	Connector 2×25 header (50pin)(50405020) [CN11(CRT)]
82	QCNCM1120AC9F	AQ		C	Connector (96pin)(50409605) [CN16(EXP BUS)]
83	QSW−Z1069ACZZ	AG		B	Switch,DIP (51505001) [SW1]
84	RCRSQ2044HCZZ	AH		B	Crystal (16MHz)(55100001) [X5]
85	RCRSP1039CCZZ	AG		B	Crystal (32.768KHz)(55100023) [X3]
86	0GM5510011 6//	AM	N	B	Crystal (20MHz) [X4]
87	RCRSQ1017ACZZ	AP		B	Crystal (1.8432MHz)(55100131) [X6]
88	RCRSQ2045HCZZ	AH		B	Crystal (14.31818MHz)(55114318) [X1]
89	RCRSP1034ACZZ	AD		B	Ceramic OSC (3.84MHz)(55200042) [X2]
	(Unit)				(PC−4602··U,Y,S,K,E)
901	DUNTK2296RHZZ	**	N	E	Main logic PWB ass'y (PC−4602··H,Q)
	DUNTK2295RHZZ	**	N	E	Main logic PWB ass'y (PC−4602··G,W)
	DUNTK2333RHZZ	**	N	E	Main logic PWB ass'y (PC−4641··U,Y,S,K,E)
	DUNTK2294RHZZ	**	N	E	Main logic PWB ass'y (PC−4641··H,Q)
	DUNTK2253RHZZ	**	N	E	Main logic PWB ass'y (PC−4641··G,W)
	DUNTK2332RHZZ	**	N	E	Main logic PWB ass'y

9 CE-451A CRT adaptor board(USA··standard,others··option)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGT1156ACZZ	AE		C	Angle
2	LX−BZ1141CCZZ	AA		C	Screw
3	MSPRP1007ACZZ	AL	N	C	Plate spring
4	PCAPH1012ACZZ	AC		C	9P cap [J1]
5	QCNCM1060AC03	AB		B	Connector(short pin)(3pin)
6	QCNCW1057ACZZ	AB		C	Connector(short socket) [CN2]
7	QCNCW1119AC0i	AK		C	Connector(9pin) [CN1]
8	QCNCW2415RC5J	AV		C	Connector(50pin) [C4~9]
9	RC−KZ1054CCZZ	AB		C	Capacitor (50WV 0.1μF) [B1~7]
10	RCŌRF6632RCZZ	AC		C	Core [X2]
11	RCRSQ2045HCZZ	AH		B	Crystal (14.31818MHz) [X1]
12	RCRSQ2046HCZZ	AH		B	Crystal (16.257MHz) [C10~13]
13	VCCCPU1HH150J	AA		C	Capacitor (50WV 15pF) [C3,14~16]
14	VCKYPU1HB102K	AA		C	Capacitor (50WV 1000pF) [C1,2]
15	VCSAVU1AE336M	AD		C	Capacitor (10WV 33μF) [IC2]
16	VHiLZ93D13/−1	AQ		B	IC (LZ93D13) [IC3]
17	VHiSC4720//−1	BE		B	IC (SC4720) [IC4,5]
18	VHiTC5563−15L	AU		B	IC (TC5563−15L) [IC6]
19	VHiT74LS244−C	AK		B	IC (T74LS244) [IC1]
20	VHi57128AAA0B	BF		B	IC (57128AAA0B) [R1]
21	VRD−RC2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%) [R2]
22	VRD−RC2EY470J	AA		C	Resistor (1/4W 47Ω ±5%)
23	XBPSD30P04000	AA		C	Screw (3×4)
101	TiNSM1021HCZZ	AD		D	Operation manual(E,F,G,S) (Option··except USA)
102	PSPAG1038ACZZ	AB		C	Rubber spacer (Option··except USA)
103	SPAKA1958ACZZ	AG		D	Packing cushion (Option··except USA)
104	SPAKC1944ACZZ	AK		D	Packing case (Option··except USA)
105	SPAKP2417HCZZ	AK		D	Vinyl bag (90×220㎜)(Option··except USA)
106	SSAKA0006UCZZ	AA		D	Vinyl bag (50×60㎜)(Option··except USA)
107	TCAUH1018ACZZ	AN		C	Caution label (Option··except USA)
108	XBSSC30P08000	AA		C	Screw/White (3×8)(Option··except USA)
109	XBSSF30P08000	AA		C	Screw/Black (3×8)(Option··except USA)
	(Unit)				(U only)
901	DUNT−2280ACZZ	BS	N	E	CRT adaptor (92133620)(This includes №1~23)

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
〔C〕				
CADPA1005AC01	3- 1	BQ		B
〔D〕				
DFLP-1134ACZZ	6- 18	BF	N	D
DUNT-2226ACZZ	1- 45	BK	N	E
〃	2- 901	BK	N	E
DUNT-2227ACZZ	1- 45	BK	N	E
〃	2- 901	BK	N	E
DUNT-2228ACZZ	1- 45	BK	N	E
〃	2- 901	BK	N	E
DUNT-2229ACZZ	1- 7	CE	N	E
DUNT-2238ACZZ	7- 1		N	E
DUNT-2239ACZZ	7- 1		N	E
DUNT-2240ACZZ	7- 1		N	E
DUNT-2241ACZZ	7- 1		N	E
DUNT-2242ACZZ	7- 1		N	E
DUNT-2280ACZZ	9- 901	BS	N	E
DUNT-2307ACZZ	1- 45	BK	N	E
〃	2- 901	BK	N	E
DUNTK2230ACSA	1- 61	BU	N	E
〃	4- 901	BU	N	E
DUNTK2230ACZZ	1- 61	BU	N	E
〃	4- 901	BU	N	E
DUNTK2231ACZZ	1- 65	**	N	D
DUNTK2232ACZZ	1- 37	CC	N	C
DUNTK2253RHZZ	1- 54	**	N	E
〃	8- 901	**	N	E
DUNTK2294RHZZ	1- 54	**	N	E
〃	8- 901	**	N	E
DUNTK2295RHZZ	1- 54	**	N	E
〃	8- 901	**	N	E
DUNTK2296RHZZ	1- 54	**	N	E
〃	8- 901	**	N	E
DUNTK2332RHZZ	1- 54	**	N	E
〃	8- 901	**	N	E
DUNTK2333RHZZ	1- 54	**	N	E
〃	8- 901	**	N	E
〔G〕				
GCASP5017SCZZ	6- 17	AE	N	D
GLEGG1019CCZZ	1- 47	AB		C
GLEGG1024CCZZ	1- 26	AA		C
〔J〕				
JHNDP1005ACSA	1- 50	AF		D
JHNDP1005ACZZ	1- 50	AF		D
JHNDP5003SCZZ	6- 10	AB		C
〔L〕				
LANGT1156ACZZ	9- 1	AE		C
LPLTP1017ACZZ	6- 12	AB		C
LX-BZ1027ACSA	1- 73	AB		C
LX-BZ1027ACZZ	1- 73	AB		C
LX-BZ1141CCZZ	1- 56	AA		C
〃	9- 2	AA		C
LX-BZ1147CCZZ	1- 36	AA		C
LX-BZ1182CCZZ	1- 62	AB		C
〔M〕				
MSPRP1007ACZZ	9- 3	AL	N	C
〔P〕				
PCAPH1012ACZZ	9- 4	AC		C
PCASZ2005HCZA	6- 15	AC		D
PCOVP6633RCZZ	5- 86	AB		C
PGUMM1562CCZZ	1- 63	AE		C
PSPAG1038ACZZ	9- 102	AB		C
PZETV1041ACZZ	1- 19	AE	N	C
PZETV1042ACZZ	1- 9	AE	N	C
PZETV1043ACZZ	1- 42	AE	N	C
〃	5- 89	AE	N	C
〔Q〕				
QCNCM00NSSC50	8- 81	AM		C
QCNCM1060AC03	9- 5	AB		B
QCNCM1120AC9F	8- 82	AQ		C
QCNCM2303SC0H	8- 74	AB		C
QCNCM2346SC4J	8- 80	AL		C
QCNCM5016SC0B	5- 69	AA		C
〃	8- 72	AA		C
QCNCM5016SC0F	8- 73	AB		C
QCNCW1057ACZZ	9- 6	AB		C
QCNCW1119AC0J	9- 7	AK		C
QCNCW2415RC5J	9- 8	AV		C
QCNW-1239ACZZ	1- 66	AB		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
QSOCZ6428ACZZ	8- 68	AE		C
QSOCZ6440ACZZ	8- 69	AG		C
QSW-P1067ACZZ	1- 35	AD		B
QSW-Z1069ACZZ	8- 83	AG		B
〔R〕				
RADPA1004ACZZ	3- 1	BP		B
〃	3- 1	BP		B
RADPA1006ACZZ	3- 1	BQ		B
〃	3- 1	BQ		B
RADPA1007ACZZ	3- 1	BP		B
〃	3- 1	BP		B
RADPA1008ACZA	3- 1	BP		B
〃	3- 1	BP		B
RADPA1009ACZZ	3- 1	BP		B
RADPA1010ACZZ	3- 1	BP		B
RADPA1011ACZZ	3- 1	BQ		B
RADPA1012ACZZ	3- 1	BQ		B
RADPA1013ACZZ	3- 1	BQ	N	B
RALMB1007HCZZ	1- 49	AK		C
RC-KZ1054CCZZ	5- 30	AB		C
〃	8- 40	AB		C
〃	9- 9	AB		C
RCORF6632RCZZ	9- 10	AC		C
RCRSP1034ACZZ	8- 89	AD		B
RCRSP1039CCZZ	8- 85	AG		B
RCRSQ1017ACZZ	8- 87	AP		B
RCRSQ2044HCZZ	8- 84	AH		B
RCRSQ2045HCZZ	8- 88	AH		B
〃	9- 11	AH		B
RCRSQ2046HCZZ	9- 12	AH		B
RMPTC4102QCJB	8- 23	AB		B
RMPTC4152QCJB	8- 25	AC	N	B
RMPTC4472QCJB	8- 27	AB		B
RMPTC4563QCJB	8- 29	AB		B
RMPTC7123QCJB	8- 24	AC	N	B
RMPTC8472QCJB	8- 26	AB	N	B
RMPTC8563QCJB	8- 28	AC		B
RVR-P1009ACZZ	5- 24	AE	N	B
〔S〕				
SPAKA1958ACZZ	9- 103	AG		D
SPAKA1982ACZZ	6- 14	AE		D
SPAKA5416SCZZ	6- 26	AB		D
SPAKC1944ACZZ	9- 104	AK		D
SPAKP2417HCZZ	9- 105	AK		D
SSAKA0006UCZZ	9- 106	AA		D
SSAKA0006WCZZ	6- 7	AB		D
SSAKA0019SCZZ	6- 3	AA		D
SSAKH0011HCZZ	6- 11	AA		D
SSAKH0015HCZZ	6- 19	AA		D
SSAKH5002CCZZ	6- 2	AA		D
〔T〕				
TCAUH1018ACZZ	9- 107	AN		C
TINSM1021HCZZ	9- 101	AD		D
TLABM1338ACZZ	6- 25	AB	N	C
TLABP1317ACSA	1- 44	AB		C
TLABP1317ACZZ	1- 44	AB		C
〔U〕				
UBATZ1003ACZA	1- 71	BA		A
〃	6- 4	BA		A
〔V〕				
VCCCPU1HH150J	9- 13	AA		C
VCCCTS1HH100J	8- 31	AA	N	C
VCCCTS1HH150J	8- 35	AA	N	C
VCCCTS1HH180J	8- 36	AA	N	C
VCCCTS1HH220J	8- 37	AA	N	C
VCCCTS1HH330J	8- 38	AA	N	C
〃	8- 38	AA	N	C
VCCCTS1HH470J	8- 39	AA		C
〃	8- 39	AA		C
VCEAEA1CW106M	8- 42	AC	N	C
VCEAEU1AW336M	5- 94	AA	N	C
VCEAEU1HW105M	5- 33	AA	N	C
〃	8- 41	AA	N	C
VCEAGU1EW476M	5- 95	AB		C
VCKYPU1HB102K	9- 14	AA		C
VCKYTS1HB102K	8- 32	AA	N	C
VCKYTS1HB103K	8- 33	AA	N	C
VCQYNU1HM473K	5- 31	AB		C
VCSAVU1AE336M	9- 15	AD		C
VCSAVU1CE476M	5- 96	AH	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VHDDSS133HV-1	8- 60	AA		B	
VHDIN4148//-1	5- 61	AA		B	
VHDISS108//-1	5- 64	AB		B	
//	8- 59	AB		B	
VHEHZ3ALL//-1	5- 62	AC		B	
VHiBA6251AF-1	8- 55	AE	N	B	
VHiLU57844P-1	8- 47	AU	N	B	
VHiLZ93D13/-1	9- 16	AQ		B	
VHiLZ93J21/-1	8- 51	BC	N	B	
VHiLZ95H12/-1	8- 50	BA	N	B	
VHiMN1280T/-1	5- 47	AE		B	
VHiM4464-12PZ	8- 46	AU	N	B	
VHiSC4720//-1	9- 17	BE		B	
VHiTC4S71F/-1	8- 44	AC		B	
VHiTC4S81F/-1	8- 45	AC		B	
VHiTC5563-15L	9- 18	AU		B	
VHiTC8566F/-1	8- 52	BB		B	
VHiT74LS244-C	9- 19	AK		B	
VHi27C51AAA0A	8- 61	BF	N	B	
VHi27C51AAA1A	8- 61	BF	N	B	
VHi57128AAA0B	9- 20	BF		B	
VHi79M12AUC-1	5- 37	AP	N	B	
VHPGL3HD43/-1	1- 34	AB		B	
VHPGL3NG43/-1	1- 33	AA		B	
VHPPW17-256A1	1- 8	BM	N	D	
VRD-HT2EY101J	5- 3	AA		C	
VRD-HT2EY102J	5- 5	AA		C	
VRD-HT2EY103J	5- 6	AA		C	
VRD-HT2EY104J	5- 7	AA		C	
VRD-HT2EY120J	5- 8	AA		C	
VRD-HT2EY122J	5- 1	AA		C	
VRD-HT2EY163J	5- 9	AA		C	
VRD-HT2EY2R2J	5- 2	AA	N	C	
VRD-HT2EY222J	5- 10	AA		C	
VRD-HT2EY224J	5- 11	AA		C	
VRD-HT2EY271J	5- 12	AA		C	
VRD-HT2EY272J	5- 14	AA	N	C	
VRD-HT2EY332J	5- 13	AA		C	
VRD-HT2EY472J	5- 15	AA		C	
VRD-HT2EY561J	5- 16	AA		C	
VRD-HT2EY562J	5- 17	AA		C	
VRD-HT2EY822J	5- 18	AA		C	
VRD-HT2HY221J	5- 4	AB		C	
VRD-RC2EY000J	8- 22	AA		C	
//	8- 22	AA		C	
//	8- 22	AA		C	
VRD-RC2EY102J	1- 25	AA		C	
VRD-RC2EY103J	9- 21	AA		C	
VRD-RC2EY470J	9- 22	AA		C	
VRNHT2EK1072F	5- 19	AA	N	C	
VRNHT2EK1241F	5- 20	AA	N	C	
VRNHT2EK4122F	5- 21	AA	N	C	
VRS-TP2BD100J	8- 1	AA		C	
VRS-TP2BD102J	8- 2	AA		C	
VRS-TP2BD103J	8- 3	AA		C	
VRS-TP2BD104F	8- 4	AA	N	C	
VRS-TP2BD104J	8- 6	AA		C	
VRS-TP2BD105J	8- 7	AA		C	
VRS-TP2BD152J	8- 8	AA		C	
VRS-TP2BD153J	8- 9	AA		C	
VRS-TP2BD222J	8- 10	AA		C	
VRS-TP2BD303F	8- 11	AA	N	C	
VRS-TP2BD333F	8- 12	AA	N	C	
VRS-TP2BD333J	8- 13	AA		C	
VRS-TP2BD392J	8- 14	AA		C	
VRS-TP2BD470J	8- 15	AA		C	
VRS-TP2BD471J	8- 16	AA		C	
VRS-TP2BD474J	8- 17	AA		C	
VRS-TP2BD560J	8- 18	AA		C	
VRS-TP2BD562J	8- 19	AA		C	
VRS-TP2BD563J	8- 20	AA		C	
//	8- 20	AA		C	
VRS-TP2BD683J	8- 21	AB		C	
VS2SA673AB/-1	5- 53	AE		B	
VS2SC2021-/-1	8- 57	AB		B	
[X]					
XBPSC30P08000	1- 46	AA		C	
XBPSD30P04000	1- 38	AA		C	
//	9- 23	AA		C	
XBPSD30P06000	1- 30	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
XBPSD30P06000	5- 67	AA		C	
XBPSD30P08000	1- 18	AA		C	
XBPSF30P08000	1- 46	AA		C	
XBSSC30P08000	9- 108	AA		C	
XBSSF30P08000	9- 109	AA		C	
XUPSD30P06000	1- 59	AA		C	
XUPSD30P08000	1- 13	AA		C	
[0]					
0CFR562761/01	2- 1	AH	N	C	
0CFR562761/02	2- 2	AH	N	C	
0CFR562761/03	2- 3	AH	N	C	
0CFR562761/04	2- 4	AH	N	C	
0CFR562761/05	2- 5	AH	N	C	
0CFR562761/06	2- 6	AH	N	C	
0CFR562761/07	2- 7	AH	N	C	
0CFR562761/08	2- 8	AH	N	C	
0CFR562761/09	2- 9	AH	N	C	
0CFR562761/10	2- 10	AH	N	C	
0CFR562761/11	2- 11	AH	N	C	
0CFR562761/12	2- 12	AH	N	C	
0CFR562761/13	2- 13	AH	N	C	
0CFR562761/14	2- 14	AH	N	C	
0CFR562761/15	2- 15	AH	N	C	
0CFR562761/16	2- 16	AH	N	C	
0CFR562761/17	2- 17	AG	N	C	
0CFR562761/18	2- 18	AG	N	C	
0CFR562761/19	2- 19	AG	N	C	
0CFR562761/20	2- 20	AG	N	C	
0CFR562761/21	2- 21	AG	N	C	
0CFR562761/22	2- 22	AG	N	C	
0CFR562761/23	2- 23	AG	N	C	
0CFR562761/24	2- 24	AG	N	C	
0CFR562761/25	2- 25	AG	N	C	
0CFR562761/26	2- 26	AG	N	C	
0CFR562761/27	2- 27	AG	N	C	
0CFR562761/28	2- 28	AG	N	C	
0CFR562761/29	2- 29	AG	N	C	
0CFR562761/30	2- 30	AG	N	C	
0CFR562761/31	2- 31	AG	N	C	
0CFR562761/32	2- 32	AG	N	C	
0CFR562761/33	2- 33	AG	N	C	
0CFR562761/34	2- 34	AG	N	C	
0CFR562761/35	2- 35	AG	N	C	
0CFR562761/36	2- 36	AG	N	C	
0CFR562761/37	2- 37	AG	N	C	
0CFR562761/38	2- 38	AG	N	C	
0CFR562761/39	2- 39	AG	N	C	
0CFR562761/40	2- 40	AG	N	C	
0CFR562761/41	2- 41	AG	N	C	
0CFR562761/42	2- 42	AG	N	C	
0CFR562761/43	2- 43	AG	N	C	
0CFR562761/44	2- 44	AG	N	C	
0CFR562761/45	2- 45	AN	N	C	
0CFR562761/46	2- 46	AH	N	C	
0CFR562761/47	2- 47	AG	N	C	
0CFR562761/48	2- 48	AG	N	C	
0CFR562761/49	2- 49	AG	N	C	
0CFR562761/50	2- 50	AG	N	C	
0CFR562761/51	2- 51	AG	N	C	
0CFR562761/52	2- 52	AG	N	C	
0CFR562761/53	2- 53	AG	N	C	
0CFR562761/54	2- 54	AG	N	C	
0CFR562761/55	2- 55	AG	N	C	
0CFR562761/56	2- 56	AG	N	C	
0CFR562761/57	2- 57	AG	N	C	
0CFR562761/58	2- 58	AH	N	C	
0CFR562761/59	2- 59	AG	N	C	
0CFR562761/60	2- 60	AG	N	C	
0CFR562761/61	2- 61	AG	N	C	
0CFR562761/62	2- 62	AG	N	C	
0CFR562761/63	2- 63	AG	N	C	
0CFR562761/64	2- 64	AG	N	C	
0CFR562761/65	2- 65	AG	N	C	
0CFR562761/66	2- 66	AG	N	C	
0CFR562761/67	2- 67	AG	N	C	
0CFR562761/68	2- 68	AG	N	C	
0CFR562761/69	2- 69	AK	N	C	
0CFR562761/70	2- 70	AG	N	C	
0CFR562761/71	2- 71	AG	N	C	
0CFR562761/72	2- 72	AG	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0CFR562761/73	2- 73	AM	N	C
0CFR562761/74	2- 74	AG	N	C
0CFR562761/75	2- 75	AH	N	C
0CFR562761/76	2- 76	AH	N	C
0CFR562761/77	2- 77	AH	N	C
0CFR562761/78	2- 78	AH	N	C
0CFR562761/79	2- 79	AG	N	C
0CFR562761/80	2- 80	AG	N	C
0CFR562761/81	2- 81	AG	N	C
0CFR562761/82	2- 82	AG	N	C
0CFR562761/83	2- 83	AG	N	C
0CFR562761/84	2- 84	AG	N	C
0CFR562761/85	2- 85	AG	N	C
0CFR562761/86	2- 86	AG	N	C
0CFR562761/87	2- 87	AG	N	C
0CFR562761/88	2- 88	AG	N	C
0CFR562761/89	2- 89	AG	N	C
0CFR562761/90	2- 90	AG	N	C
0CFR562762/01	2- 1	AH	N	C
0CFR562762/02	2- 2	AH	N	C
0CFR562762/03	2- 3	AH	N	C
0CFR562762/04	2- 4	AH	N	C
0CFR562762/05	2- 5	AH	N	C
0CFR562762/06	2- 6	AH	N	C
0CFR562762/07	2- 7	AH	N	C
0CFR562762/08	2- 8	AH	N	C
0CFR562762/09	2- 9	AH	N	C
0CFR562762/10	2- 10	AH	N	C
0CFR562762/11	2- 11	AH	N	C
0CFR562762/12	2- 12	AH	N	C
0CFR562762/13	2- 13	AH	N	C
0CFR562762/14	2- 14	AH	N	C
0CFR562762/15	2- 15	AH	N	C
0CFR562762/16	2- 16	AH	N	C
0CFR562762/17	2- 17	AG	N	C
0CFR562762/18	2- 18	AG	N	C
0CFR562762/19	2- 19	AG	N	C
0CFR562762/20	2- 20	AG	N	C
0CFR562762/21	2- 21	AG	N	C
0CFR562762/22	2- 22	AG	N	C
0CFR562762/23	2- 23	AG	N	C
0CFR562762/24	2- 24	AG	N	C
0CFR562762/25	2- 25	AG	N	C
0CFR562762/26	2- 26	AG	N	C
0CFR562762/27	2- 27	AG	N	C
0CFR562762/28	2- 28	AG	N	C
0CFR562762/29	2- 29	AG	N	C
0CFR562762/30	2- 30	AG	N	C
0CFR562762/31	2- 31	AG	N	C
0CFR562762/32	2- 32	AG	N	C
0CFR562762/33	2- 33	AG	N	C
0CFR562762/34	2- 34	AG	N	C
0CFR562762/35	2- 35	AG	N	C
0CFR562762/36	2- 36	AG	N	C
0CFR562762/37	2- 37	AG	N	C
0CFR562762/38	2- 38	AG	N	C
0CFR562762/39	2- 39	AG	N	C
0CFR562762/40	2- 40	AG	N	C
0CFR562762/41	2- 41	AG	N	C
0CFR562762/42	2- 42	AG	N	C
0CFR562762/43	2- 43	AG	N	C
0CFR562762/44	2- 44	AG	N	C
0CFR562762/45	2- 45	AN	N	C
0CFR562762/46	2- 46	AH	N	C
0CFR562762/47	2- 47	AG	N	C
0CFR562762/48	2- 48	AG	N	C
0CFR562762/49	2- 49	AG	N	C
0CFR562762/50	2- 50	AG	N	C
0CFR562762/51	2- 51	AG	N	C
0CFR562762/52	2- 52	AG	N	C
0CFR562762/53	2- 53	AG	N	C
0CFR562762/54	2- 54	AG	N	C
0CFR562762/55	2- 55	AG	N	C
0CFR562762/56	2- 56	AG	N	C
0CFR562762/57	2- 57	AG	N	C
0CFR562762/58	2- 58	AH	N	C
0CFR562762/59	2- 59	AG	N	C
0CFR562762/60	2- 60	AG	N	C
0CFR562762/61	2- 61	AG	N	C
0CFR562762/62	2- 62	AG	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0CFR562762/63	2- 63	AG	N	C
0CFR562762/64	2- 64	AG	N	C
0CFR562762/65	2- 65	AG	N	C
0CFR562762/66	2- 66	AG	N	C
0CFR562762/67	2- 67	AG	N	C
0CFR562762/68	2- 68	AG	N	C
0CFR562762/69	2- 69	AK	N	C
0CFR562762/70	2- 70	AG	N	C
0CFR562762/71	2- 71	AG	N	C
0CFR562762/72	2- 72	AG	N	C
0CFR562762/73	2- 73	AM	N	C
0CFR562762/74	2- 74	AG	N	C
0CFR562762/75	2- 75	AH	N	C
0CFR562762/76	2- 76	AH	N	C
0CFR562762/77	2- 77	AH	N	C
0CFR562762/78	2- 78	AH	N	C
0CFR562762/79	2- 79	AG	N	C
0CFR562762/80	2- 80	AG	N	C
0CFR562762/81	2- 81	AG	N	C
0CFR562762/82	2- 82	AG	N	C
0CFR562762/83	2- 83	AG	N	C
0CFR562762/84	2- 84	AG	N	C
0CFR562762/85	2- 85	AG	N	C
0CFR562762/86	2- 86	AG	N	C
0CFR562762/87	2- 87	AG	N	C
0CFR562762/88	2- 88	AG	N	C
0CFR562762/89	2- 89	AG	N	C
0CFR562762/90	2- 90	AG	N	C
0CFR562763/01	2- 1	AH	N	C
0CFR562763/02	2- 2	AH	N	C
0CFR562763/03	2- 3	AH	N	C
0CFR562763/04	2- 4	AH	N	C
0CFR562763/05	2- 5	AH	N	C
0CFR562763/06	2- 6	AH	N	C
0CFR562763/07	2- 7	AH	N	C
0CFR562763/08	2- 8	AH	N	C
0CFR562763/09	2- 9	AH	N	C
0CFR562763/10	2- 10	AH	N	C
0CFR562763/11	2- 11	AH	N	C
0CFR562763/12	2- 12	AH	N	C
0CFR562763/13	2- 13	AH	N	C
0CFR562763/14	2- 14	AH	N	C
0CFR562763/15	2- 15	AH	N	C
0CFR562763/16	2- 16	AH	N	C
0CFR562763/17	2- 17	AG	N	C
0CFR562763/18	2- 18	AG	N	C
0CFR562763/19	2- 19	AG	N	C
0CFR562763/20	2- 20	AG	N	C
0CFR562763/21	2- 21	AG	N	C
0CFR562763/22	2- 22	AG	N	C
0CFR562763/23	2- 23	AG	N	C
0CFR562763/24	2- 24	AG	N	C
0CFR562763/25	2- 25	AG	N	C
0CFR562763/26	2- 26	AG	N	C
0CFR562763/27	2- 27	AG	N	C
0CFR562763/28	2- 28	AG	N	C
0CFR562763/29	2- 29	AG	N	C
0CFR562763/30	2- 30	AG	N	C
0CFR562763/31	2- 31	AG	N	C
0CFR562763/32	2- 32	AG	N	C
0CFR562763/33	2- 33	AG	N	C
0CFR562763/34	2- 34	AG	N	C
0CFR562763/35	2- 35	AG	N	C
0CFR562763/36	2- 36	AG	N	C
0CFR562763/37	2- 37	AG	N	C
0CFR562763/38	2- 38	AG	N	C
0CFR562763/39	2- 39	AG	N	C
0CFR562763/40	2- 40	AG	N	C
0CFR562763/41	2- 41	AG	N	C
0CFR562763/42	2- 42	AG	N	C
0CFR562763/43	2- 43	AG	N	C
0CFR562763/44	2- 44	AG	N	C
0CFR562763/45	2- 45	AN	N	C
0CFR562763/46	2- 46	AH	N	C
0CFR562763/47	2- 47	AG	N	C
0CFR562763/48	2- 48	AG	N	C
0CFR562763/49	2- 49	AG	N	C
0CFR562763/50	2- 50	AG	N	C
0CFR562763/51	2- 51	AG	N	C
0CFR562763/52	2- 52	AG	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
0CFR562763/53	2- 53	AG	N	C	
0CFR562763/54	2- 54	AG	N	C	
0CFR562763/55	2- 55	AG	N	C	
0CFR562763/56	2- 56	AG	N	C	
0CFR562763/57	2- 57	AG	N	C	
0CFR562763/58	2- 58	AH	N	C	
0CFR562763/59	2- 59	AG	N	C	
0CFR562763/60	2- 60	AG	N	C	
0CFR562763/61	2- 61	AG	N	C	
0CFR562763/62	2- 62	AG	N	C	
0CFR562763/63	2- 63	AG	N	C	
0CFR562763/64	2- 64	AG	N	C	
0CFR562763/65	2- 65	AG	N	C	
0CFR562763/66	2- 66	AG	N	C	
0CFR562763/67	2- 67	AG	N	C	
0CFR562763/68	2- 68	AG	N	C	
0CFR562763/69	2- 69	AK	N	C	
0CFR562763/70	2- 70	AG	N	C	
0CFR562763/71	2- 71	AG	N	C	
0CFR562763/72	2- 72	AG	N	C	
0CFR562763/73	2- 73	AM	N	C	
0CFR562763/74	2- 74	AG	N	C	
0CFR562763/75	2- 75	AH	N	C	
0CFR562763/76	2- 76	AH	N	C	
0CFR562763/77	2- 77	AH	N	C	
0CFR562763/78	2- 78	AH	N	C	
0CFR562763/79	2- 79	AG	N	C	
0CFR562763/80	2- 80	AG	N	C	
0CFR562763/81	2- 81	AG	N	C	
0CFR562763/82	2- 82	AG	N	C	
0CFR562763/83	2- 83	AG	N	C	
0CFR562763/84	2- 84	AG	N	C	
0CFR562763/85	2- 85	AG	N	C	
0CFR562763/86	2- 86	AG	N	C	
0CFR562763/87	2- 87	AG	N	C	
0CFR562763/88	2- 88	AG	N	C	
0CFR562763/89	2- 89	AG	N	C	
0CFR562763/90	2- 90	AG	N	C	
0CFR562830-01	2- 1	AH	N	C	
0CFR562830-02	2- 2	AH	N	C	
0CFR562830-03	2- 3	AH	N	C	
0CFR562830-04	2- 4	AH	N	C	
0CFR562830-05	2- 5	AH	N	C	
0CFR562830-06	2- 6	AH	N	C	
0CFR562830-07	2- 7	AH	N	C	
0CFR562830-08	2- 8	AH	N	C	
0CFR562830-09	2- 9	AH	N	C	
0CFR562830-10	2- 10	AH	N	C	
0CFR562830-11	2- 11	AH	N	C	
0CFR562830-12	2- 12	AH	N	C	
0CFR562830-13	2- 13	AH	N	C	
0CFR562830-14	2- 14	AH	N	C	
0CFR562830-15	2- 15	AH	N	C	
0CFR562830-16	2- 16	AH	N	C	
0CFR562830-17	2- 17	AG	N	C	
0CFR562830-18	2- 18	AG	N	C	
0CFR562830-19	2- 19	AG	N	C	
0CFR562830-20	2- 20	AG	N	C	
0CFR562830-21	2- 21	AG	N	C	
0CFR562830-22	2- 22	AG	N	C	
0CFR562830-23	2- 23	AG	N	C	
0CFR562830-24	2- 24	AG	N	C	
0CFR562830-25	2- 25	AG	N	C	
0CFR562830-26	2- 26	AG	N	C	
0CFR562830-27	2- 27	AG	N	C	
0CFR562830-28	2- 28	AG	N	C	
0CFR562830-29	2- 29	AG	N	C	
0CFR562830-30	2- 30	AG	N	C	
0CFR562830-31	2- 31	AG	N	C	
0CFR562830-32	2- 32	AG	N	C	
0CFR562830-33	2- 33	AG	N	C	
0CFR562830-34	2- 34	AG	N	C	
0CFR562830-35	2- 35	AG	N	C	
0CFR562830-36	2- 36	AG	N	C	
0CFR562830-37	2- 37	AG	N	C	
0CFR562830-38	2- 38	AG	N	C	
0CFR562830-39	2- 39	AG	N	C	
0CFR562830-40	2- 40	AG	N	C	
0CFR562830-41	2- 41	AG	N	C	
0CFR562830-42	2- 42	AG	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
0CFR562830-43	2- 43	AG	N	C	
0CFR562830-44	2- 44	AG	N	C	
0CFR562830-45	2- 45	AN	N	C	
0CFR562830-46	2- 46	AH	N	C	
0CFR562830-47	2- 47	AG	N	C	
0CFR562830-48	2- 48	AG	N	C	
0CFR562830-49	2- 49	AG	N	C	
0CFR562830-50	2- 50	AG	N	C	
0CFR562830-51	2- 51	AG	N	C	
0CFR562830-52	2- 52	AG	N	C	
0CFR562830-53	2- 53	AG	N	C	
0CFR562830-54	2- 54	AG	N	C	
0CFR562830-55	2- 55	AG	N	C	
0CFR562830-56	2- 56	AG	N	C	
0CFR562830-57	2- 57	AG	N	C	
0CFR562830-58	2- 58	AH	N	C	
0CFR562830-59	2- 59	AG	N	C	
0CFR562830-60	2- 60	AG	N	C	
0CFR562830-61	2- 61	AG	N	C	
0CFR562830-62	2- 62	AG	N	C	
0CFR562830-63	2- 63	AG	N	C	
0CFR562830-64	2- 64	AG	N	C	
0CFR562830-65	2- 65	AG	N	C	
0CFR562830-66	2- 66	AG	N	C	
0CFR562830-67	2- 67	AG	N	C	
0CFR562830-68	2- 68	AG	N	C	
0CFR562830-69	2- 69	AK	N	C	
0CFR562830-70	2- 70	AG	N	C	
0CFR562830-71	2- 71	AG	N	C	
0CFR562830-72	2- 72	AG	N	C	
0CFR562830-73	2- 73	AM	N	C	
0CFR562830-74	2- 74	AG	N	C	
0CFR562830-75	2- 75	AH	N	C	
0CFR562830-76	2- 76	AH	N	C	
0CFR562830-77	2- 77	AH	N	C	
0CFR562830-78	2- 78	AH	N	C	
0CFR562830-79	2- 79	AG	N	C	
0CFR562830-80	2- 80	AG	N	C	
0CFR562830-81	2- 81	AG	N	C	
0CFR562830-82	2- 82	AG	N	C	
0CFR562830-83	2- 83	AG	N	C	
0CFR562830-84	2- 84	AG	N	C	
0CFR562830-85	2- 85	AG	N	C	
0CFR562830-86	2- 86	AG	N	C	
0CFR562830-87	2- 87	AG	N	C	
0CFR562830-88	2- 88	AG	N	C	
0CFR562830-89	2- 89	AG	N	C	
0CFR562830-90	2- 90	AG	N	C	
0CF56A185F///	2- 102	AA		C	
0CF56A514B///	2- 107	AK	N	C	
0CF56B036A///	2- 103	AQ	N	C	
0CF56B036B///	2- 103	AQ	N	C	
0CF56H089A///	2- 106	BD	N	C	
0CF56H089B///	2- 106	BD	N	C	
0CF560088B///	2- 109	AA		C	
0CF560940A///	2- 111	AA		C	
0CF561565A///	2- 110	AA		C	
0CF564965C///	2- 108	AA		C	
0CF565033M///	2- 112	AD	N	B	
0CF565524B///	2- 105	AB	N	C	
0CF565665A///	2- 104	AB		C	
0CF567664C///	2- 101	AA	N	C	
0CF567664D///	2- 114	AA	N	C	
0CF567955A///	2- 113	AA	N	C	
0GM1335//////	1- 41	BZ	N	E	
//	5- 901	BZ	N	E	
0GM13362950//	5- 22	AD	N	C	
0GM14147051//	8- 30	AM	N	B	
0GM18120220//	5- 23	AF	N	C	
0GM18130301//	5- 25	AF	N	C	
0GM18150202//	5- 26	AF	N	B	
0GM20210359//	5- 27	AB	N	C	
0GM20210486//	8- 34	AC	N	C	
//	8- 34	AC	N	C	
0GM20247302//	5- 28	AB	N	C	
0GM20256105//	5- 29	AB	N	C	
0GM24122800//	5- 32	AG	N	C	
0GM24210618//	5- 34	AC	N	C	
0GM24210631//	5- 35	AC	N	C	
0GM24210827//	5- 36	AD	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0GM24222619//	5- 38	AC	N	C
0GM24222702//	5- 39	AB	N	C
0GM24233603//	5- 40	AB	N	C
0GM24233611//	5- 41	AC	N	C
0GM24233612//	5- 42	AC	N	C
0GM24247501//	5- 43	AB	N	C
0GM24247715//	5- 44	AB	N	C
0GM30274383//	8- 43	AE	N	B
0GM30870201//	8- 48	BU	N	B
0GM30882503//	8- 49	BK	N	B
0GM31104310//	5- 45	AF	N	B
0GM31110700//	5- 46	BB	N	B
0GM31179052//	5- 48	AF	N	B
0GM31514886//	8- 53	AQ	N	B
0GM31514894//	8- 54	AQ	N	B
0GM31904311//	8- 56	AF	N	B
0GM32102000//	5- 49	AG	N	B
0GM32112131//	5- 50	AC	N	B
0GM32127120//	8- 58	AB	N	B
0GM32180500//	5- 51	AB	N	B
0GM32204505//	5- 52	AL	N	B
0GM32214430//	5- 54	AP	N	B
0GM32214440//	5- 55	AQ	N	B
0GM32285500//	5- 56	AB	N	B
0GM33101004//	5- 57	AB	N	B
0GM33101040//	5- 58	AR	N	B
0GM33103035//	5- 59	AH	N	B
0GM33105301//	5- 60	AQ	N	B
0GM33352290//	5- 63	AB	N	B
0GM33352501//	5- 65	AB	N	B
0GM37641253//	8- 62	AG	N	B
0GM37641573//	8- 63	AG	N	B
0GM37674003//	8- 64	AF	N	B
0GM37674043//	8- 65	AE	N	B
0GM37674323//	8- 66	AF	N	B
0GM40133500//	1- 40	AL	N	C
//	5- 66	AL	N	C
0GM40133600//	1- 17	AC	N	C
0GM40133604//	1- 29	AD	N	C
0GM40133605//	1- 55	AG	N	C
0GM40133606//	1- 64	AP	N	C
0GM40133607//	6- 20	AF	N	C
0GM40133610//	1- 51	AD	N	C
0GM40133611//	1- 76	AC	N	C
0GM40133612//	1- 76	AC	N	C
0GM41100611//	6- 21	AA	N	C
0GM41100613//	1- 69	AD	N	C
0GM42200085//	5- 68	AA	N	C
0GM44700065//	1- 3	AC	N	C
0GM50102500//	8- 67	AK	N	C
0GM50300917//	8- 70	AK	N	C
0GM50302518//	8- 71	AN	N	C
0GM50400364//	5- 70	AC	N	C
0GM50401414//	8- 75	AD	N	C
0GM50402625//	8- 76	AE	N	C
0GM50402627//	5- 71	AN	N	C
0GM50403433//	8- 77	AM	N	C
0GM50403434//	8- 78	AQ	N	C
0GM50403435//	8- 79	AF	N	C
0GM50700007//	5- 72	AD	N	C
0GM51400006//	5- 73	AM	N	C
0GM52100030//	5- 74	AC	N	C
0GM52100171//	5- 75	AF	N	C
0GM52113351//	5- 76	AH	N	C
0GM52113352//	5- 77	AM	N	C
0GM52313353//	5- 78	AQ	N	B
0GM52313354//	5- 79	AP	N	B
0GM52313355//	5- 80	AG	N	B
0GM52313356//	5- 81	AT	N	B
0GM53113350//	5- 82	AD	N	A
0GM54300020//	1- 68	BC	N	B
0GM55100116//	8- 86	AM	N	B
0GM57113350//	5- 83	AA	N	C
0GM57113351//	5- 84	AA	N	C
0GM60201508//	1- 12	AD	N	C
0GM60201509//	6- 24	AD	N	C
0GM60201510//	6- 24	AB	N	C
0GM60201513//	1- 52	AD	N	C
0GM60201514//	1- 52	AD	N	C
0GM60201515//	1- 21	AE	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0GM60201516//	1- 21	AE	N	C
0GM60201517//	1- 23	AF	N	C
0GM60201518//	1- 23	AF	N	C
0GM60201519//	1- 23	AF	N	C
0GM60201520//	1- 23	AF	N	C
0GM60201522//	6- 27	AC	N	C
0GM60201524//	6- 22	AB	N	C
0GM60201530//	6- 16	AC	N	C
0GM60201541//	1- 22	AH	N	C
0GM60261540//	1- 27	AB	N	C
0GM60300121//	6- 13	AX	N	D
0GM60300122//	6- 13	BG	N	D
0GM60300123//	6- 13	BA	N	D
0GM60300124//	6- 23	AG	N	C
0GM61336001//	6- 8	AK	N	D
0GM61336002//	6- 6	AK	N	D
0GM61336003//	6- 5	AK	N	D
0GM61400728//	6- 1	AC	N	D
0GM61501015//	6- 101	AK	N	D
0GM61501016//	6- 9	AN	N	D
0GM61501017//	6- 9	AS	N	D
0GM61501018//	6- 101	AK	N	D
0GM61501019//	6- 9	AN	N	D
0GM61501020//	6- 9	AS	N	D
0GM70113360//	1- 32	AC	N	C
0GM70113361//	1- 75	AC	N	C
//	5- 85	AC	N	B
0GM73133601//	1- 48	BC	N	D
0GM73133602//	1- 28	BE	N	D
0GM73133603//	1- 1	BA	N	D
0GM73133604//	1- 20	AW	N	D
0GM73133605//	1- 72	AN	N	C
0GM73133606//	1- 2	AC	N	C
0GM73133607//	1- 4	AC	N	C
0GM73133609//	1- 14	AD	N	C
0GM73133611//	1- 48	BC	N	D
0GM73133612//	1- 28	BE	N	D
0GM73133613//	1- 1	BA	N	D
0GM73133614//	1- 20	AW	N	D
0GM73133615//	1- 72	AN	N	C
0GM73133616//	1- 2	AC	N	C
0GM73133617//	1- 4	AC	N	C
0GM73133619//	1- 14	AD	N	C
0GM81000002//	5- 87	AB	N	C
0GM81100051//	1- 5	AD	N	C
0GM81200102//	1- 24	AD	N	C
0GM81300012//	5- 88	AC	N	C
0GM81300095//	1- 67	AB	N	C
0GM81400081//	1- 39	AH	N	C
0GM81600012//	1- 58	AD	N	C
0GM81600013//	1- 57	AD	N	C
0GM91133623//	1- 6	AZ	N	C
0GM92126219//	1- 31	AE	N	C
0GM92130811//	1- 53	AD	N	C
0GM92133502//	5- 90	AG	N	C
0GM92133510//	5- 91	AC	N	C
0GM92133600//	1- 43	AW	N	C
//	5- 92	AW	N	C
0GM92133603//	1- 15	AT	N	C
0GM92133604//	1- 16	AT	N	C
0GM92133670//	1- 74	AY	N	C
0GM92133756//	1- 60	AY	N	C
0GM99100000//	5- 93	AA	N	C
00G1473403432	4- 7	BM	N	E
00G1476943000	4- 5	AY	N	E
00G1490051603	4- 101	CP	N	D
00G1490051701	4- 102	CE	N	D
00G1553211005	4- 6	BL	N	E
00G1678803909	4- 1	AC	N	D
00G1678803910	4- 1	AC	N	D
00G17967693//	4- 3	AH	N	E
00G1796769609	4- 2	AH	N	D
00G1796769610	4- 2	AH	N	D
00G1796772900	4- 4	BP	N	E

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